JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

ELECTRICAL AND ELECTRONICS ENGINEERING

Course Code	ANALOG ELECTRONIC CIRCUITS		L	T	P	C
20A04404T			3	0	0	3
Pre-requisite	Network Analysis, Electronic Devices and Circuits	Semester	IV			

Course Objectives:

- List various types of feedback amplifiers, oscillators and large signal Amplifiers.
- Explain the operation of various electronic circuits and linear ICs.
- Apply various types of electronic circuits to solve engineering problems
- Analyse various electronic circuits and regulated power supplies for proper understanding
- Justify choice of transistor configuration in a cascade amplifier.
- Design electronic circuits for a given specification.

Course Outcomes (CO):

CO1. List various types of feedback amplifiers, oscillators and large signal amplifiers
CO2. Explain the operation of various electronic circuits and linear ICs
CO3. Apply various types of electronic circuits to solve engineering problems
CO4. Analyze various electronic circuits and regulated power supplies for proper understanding
CO5. Justify choice of transistor configuration in a cascade amplifier
CO6. Design electronic circuits for a given specification

UNIT - I	Multistage Amplifiers

Classification of amplifiers, different coupling schemes used in amplifiers, general analysis of cascade amplifiers, Choice of transistor configuration in a cascade amplifier, frequency response and analysis of two stage RC coupled and direct coupled amplifiers, principles of Darlington amplifier, Cascode amplifier.

UNIT - II	Feedback Amplifiers and Oscillators

Concepts of Feedback, Classification of Feedback Amplifiers, Transfer Gain with Feedback, General Characteristics of Negative-Feedback Amplifiers, Effect of Feedback on Amplifier characteristics, Analysis of a feedback Amplifiers - Voltage – Series, Current-Series, Current-shunt and Voltage–shunt.
Oscillators: Sinusoidal Oscillators, Conditions for oscillations, Phase-shift Oscillator, Wien Bridge Oscillator, L-C Oscillators (Hartley and Colpitts).

UNIT - III	Large Signal Amplifiers (Power Amplifiers)

Introduction, Classification, Class A large signal amplifiers, Second - Harmonic Distortion, Higher - Order Harmonic Generations, Transformer Coupled Class A Audio Power Amplifier, Efficiency of Class A, Class B, Class AB Amplifiers, Distortion in Power Amplifiers, Class C Power Amplifier.

UNIT - IV	Operational Amplifier

Introduction, Block diagram, Characteristics and Equivalent circuits of an ideal op-amp, Various types of Operational Amplifiers and their applications, Power supply configurations for OP-AMP applications, Inverting and non-inverting amplifier configurations. The Practical op-amp: Introduction, Input offset voltage, Offset current, Thermal drift, Effect of variation in power supply voltage, common-mode rejection ratio, Slew rate and its Effect, PSRR and Gain–bandwidth product, frequency limitations and compensations, transient response.

UNIT - V	Applications of OP-AMPs and Special ICs

Adder, Integrator, Differentiator, Difference amplifier and Instrumentation amplifier, Converters: Current to voltage and voltage to current converters, Active Filters: First order filters, second order low pass, high pass, band pass and band reject filters, Oscillators: RC phase shift oscillator, Wien bridge oscillator, Square wave generator.
Special Purpose Integrated Circuits: Functional block diagram, working, design and applications of

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ELECTRICAL AND ELECTRONICS ENGINEERING

Timer 555 (Monostable & Astable), Functional block diagram, working and applications of VCO566, PLL565, Fixed and variable Voltage regulators.
Textbooks:
• Millman, Halkias and Jit , "Electronic Devices and Circuits" , 4th Edition , McGraw Hill Education (India) Private Ltd.,2015. • Salivahanan and N. Suresh Kumar, " Electronic Devices and Circuits",4thEdition,McGrawHill Education(India)Private Ltd.,2017. • Ramakanth A. Gayakwad, "Op-Amps& LinearICs",4thEdition, Pearson, 2017.
Reference Books:
• Millman and Taub, Pulse, Digital and Switching Waveforms, 3rdEdition, TataMcGraw-Hill Education, 2011. • J. Milliman, C.C. Halkias and Chetan Parikh, "Integrated Electronics", 2ndEdition, McGraw Hill, 2010. • David A. Bell, " Electronic Devices and Circuits", 5thedition,OxfordPress,2008. • D. Roy Choudhury, "LinearIntegratedCircuits",2ndEdition, New Age International (p)Ltd,2003.

UNIT I

MULTI STAGE AMPLIFIERS

Amplifier:

An Amplifier is an electronic circuit that increases the amplitude of a given input signal. i.e the amplifier is used to obtain a larger ac signal output from the small given input signal.

In general BJTs and FETs are commonly used as amplifying elements.

The frequency of the amplifier output must be same as that of the frequency of the amplifier input. If we assume the sinusoidal signal as an input of the amplifier, the output should also be a sinusoidal with the same frequency as that of the input signal.

Classification of Amplifiers:

The Amplifiers can be classified in different ways as discussed below.

1) Based on frequency range:
   - i) Audio frequency Amplifiers (20HZ - 20KHZ)
   - ii) Radio frequency Amplifiers (>20kHz)
   - iii) Video Frequency Amplifiers (5-8 MHz)
   - iv) Very Low Frequency Amplifiers (VLF) (10KHZ - 30KHZ)
   - v) Low Frequency Amplifiers (LF) (30KHZ - 300kHz)
   - vi) Medium Frequency Amplifiers (300KHZ - 3000 kHz)
   - vii) High Frequency Amplifiers (3MHZ - 30MHZ)
   - viii) Very High Frequency Amplifiers (30MHZ - 300MHZ)
   - ix) Ultra High Frequency Amplifiers (300MHZ - 3000MHZ)
   - x) Super High Frequency Amplifiers (3000MAZ - 30,000 MHZ)

2) Based on the method of operation:

i) Class A Amplifier: An amplifier is said to be Class A amplifier if the Q point and the input signal are selected such that the output signal is obtained for full input signal.

For this amplifier the position of the Q-point is approximately at the middle of the dc load line.

ii) Class B amplifier: An amplifier is said to be class B amplifier if the Q-point and input signal are selected such that the output signal is obtained for only one half cycle of the full input cycle.

iii) Class-AB Amplifier: An amplifier is said to be class AB amplifier if the Q-point and the input signal are selected such that the output signal is obtained for more than 180° and less than 360° of the full input cycle.

iv) Class-C Amplifier: An Amplifier is said to be class-c amplifier if the Q-Point and the input signal are selected such that the output signal is obtained for less than half cycle of full input cycle.

3) Based on the method of Coupling:

i) RC Coupled Amplifier: Resistors and Capacitors are used as Coupling Components. They block DC and gives flat response at mid frequencies.

ii) Transformer Coupled Amplifier: Transformer is used as a Coupling Component. It provides impedance matching.

iii) Direct Coupled Amplifier: If the output of the first stage is directly connected to the input of the next stage without using any component, that amplifier is known as direct coupled amplifier It does not block DC signal components.

4) Based on the type of the Load:

i) Resistive Load Amplifier ii) Inductive Load Amplifier

5) Based on the type of the signal being handled:

Based on the level of the signal, signals are two types. They are small signal and large signal. So the amplifiers are categorised as i) Small signal amplifier ii) Large signal Amplifier.

6) Based on the type of application:

i) voltage amplifier: Amplifies voltage of the input signal.

ii) Current amplifier: Amplifies current of the input signal.

iii) power amplifier: Amplifies both voltage and current of the input signal.

iv) Tuned amplifier: Amplifier of this kind is used for impedance matching.

7) Based on the type of active device used:

i) BJT amplifier ii) FET Amplifier

8) Based on the transistor Configuration: a) under BJT

i) Common Emitter Amplifier ii) Common Base Amplifier

iii) Common Collector Amplifier.

b) under FET

i) Common Source amplifier ii) Common drain amplifier

iii) Common Gate amplifier.

9) According to the number of stages:

i) Single stage Amplifier ii) Multistage Amplifier

Hybrid model (or) h-parameter model for a general two port network:

The h-parameter equations for a general two port network are given as

$$V_1 = h_i I_1 + h_r V_2$$

$$I_2 = h_f I_1 + h_o V_2$$

The h-parameter model that satisfies the above two equations can be verified by applying KVL in the input loop and KCL at the output node, for the following figure.

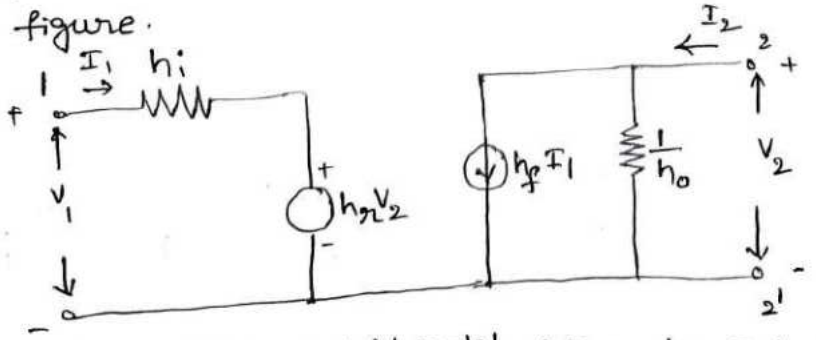


fig: Hybrid model for a two port network.

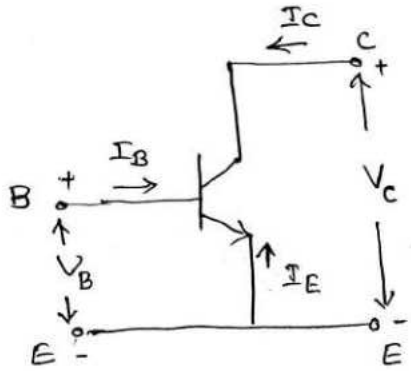
NOTE: Transistor is a type of two port network. So the H-parameter model given in the above figure can be applied for a transistor also. The notations for V_1, I_1 and V_2, I_2 will be changed based on the configuration in which the transistor is connected in. And also h_i, h_r, h_f and h_o notations are changed based on the configurations.

Hybrid model for the transistor in three different Configurations:

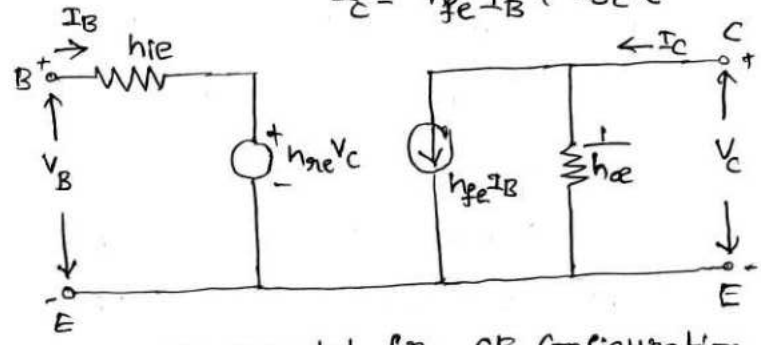
a) Common Emitter Configuration:

For common emitter the H-parameter equations are $V_B = h_{ie} I_B + h_{re} V_C$

$I_C = h_{fe} I_B + h_{oe} V_C$



fig(a) CE configuration

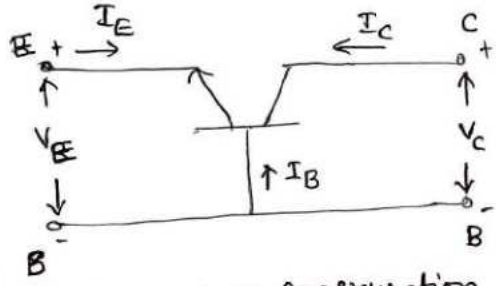


fig(b): Hybrid model for CE configuration

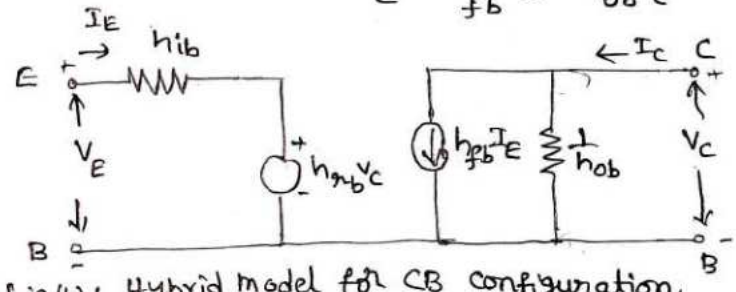
b) Common Base Configuration:

For common base the H-parameter equations are $V_E = h_{ib} I_E + h_{rb} V_C$

$I_C = h_{fb} I_E + h_{ob} V_C$



fig(a) Common base configuration

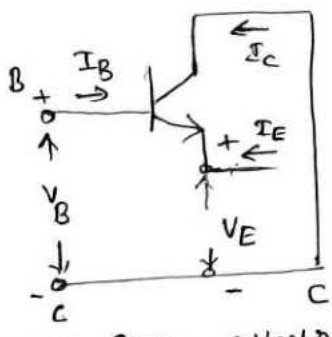


fig(b): Hybrid model for CB configuration.

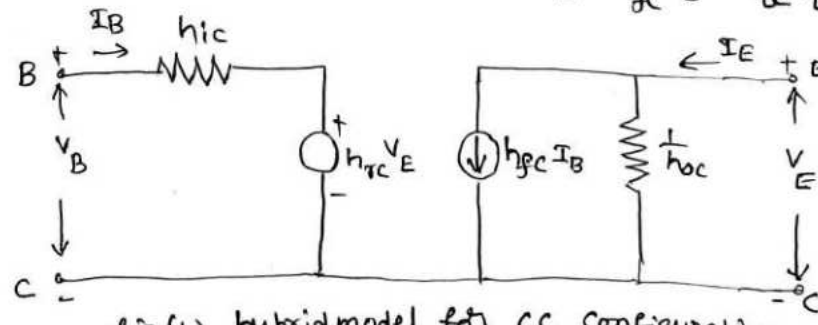
c) Common collector configuration:

For common collector the H-parameter equations are $V_B = h_{ic} I_B + h_{rc} V_E$

$I_E = h_{fc} I_B + h_{oc} V_E$



fig(a) Common collector configuration



fig(b) hybrid model for CC configuration.

Small signal Analysis of a generalized transistor amplifier:

To form a transistor amplifier it is necessary to connect an external load, source of a signal along with proper biasing for transistor network. The transistor can be connected in any one of the three possible configurations.

The basic transistor amplifier and it's generalized h-parameter model are shown in below using exact model.

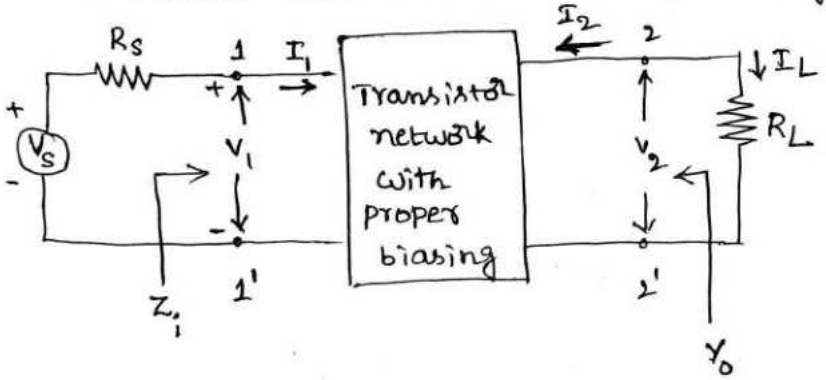


fig: Basic Amplifier using transistor

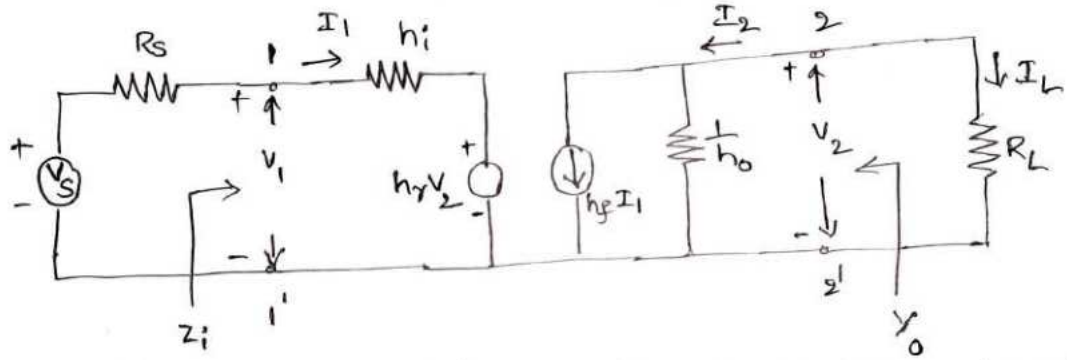


fig: Generalized h-parameter model for a transistor amplifier

To analyse the hybrid model we need to find the parameters such as Current Gain (A_I), Input Impedance (Z_i), Voltage Gain (A_V), output Admittance (Y_o), current Gain with Source (A_{IS}), voltage gain with source (A_{VS}) and power gain. Let us derive them one by one.

Current Gain (A_I):

$$\text{current Gain } (A_I) = \frac{I_L}{I_1} = -\frac{I_2}{I_1} \qquad (\because \text{from the figure } I_L = -I_2)$$

we know that $I_2 = h_f I_1 + h_o V_2$

$$\Rightarrow I_2 = h_f I_1 + h_o(-I_2 R_L) \qquad (\because \text{from figure } V_2 = I_L R_L = -I_2 R_L)$$

$$\Rightarrow I_2 (1 + h_o R_L) = h_f I_1$$

$$\Rightarrow \frac{I_2}{I_1} = \frac{h_f}{1+h_o R_L}$$

$$\Rightarrow \frac{-I_2}{I_1} = \frac{-h_f}{1+h_o R_L}$$

$$\therefore \boxed{A_I = \frac{-h_f}{1+h_o R_L}}$$

Input Impedance (Z_i):

Input Impedance $z_i = \frac{V_1}{I_1}$

we know that $V_1 = h_i I_1 + h_r V_2$

$$\Rightarrow V_1 = h_i I_1 + h_r(-I_2 R_L)$$

$$\Rightarrow V_1 = h_i I_1 + h_r(A_I I_1) R_L \qquad \left(\because \frac{-I_2}{I_1} = A_I \Rightarrow -I_2 = A_I I_1\right)$$

$$\Rightarrow V_1 = I_1(h_i + h_r A_I R_L)$$

$$\Rightarrow \frac{V_1}{I_1} = h_i + h_r A_I R_L$$

$$\therefore \boxed{Z_i = h_i + h_r A_I R_L}$$

Replacing $A_I = \frac{-h_f}{1+h_o R_L}$ we get $Z_i = h_i + h_r\left(\frac{-h_f}{1+h_o R_L}\right) R_L$

$$\therefore \boxed{Z_i = h_i - \frac{h_r h_f R_L}{1+h_o R_L}}$$

Voltage Gain (A_V):

Voltage Gain $A_V = \frac{V_2}{V_1}$

$$= \frac{-I_2 R_L}{V_1}$$

$$= \frac{(A_I I_1) R_L}{V_1} \qquad \left(\because A_I = \frac{-I_2}{I_1} \Rightarrow -I_2 = A_I I_1\right)$$

$$\therefore \boxed{A_V = \frac{A_I R_L}{Z_i}} \qquad \left(\because \frac{V_1}{I_1} = Z_i\right)$$

Output Admittance (Y_o):

output admittance $(Y_o) = \frac{I_2}{V_2}$ with $V_s = 0$

we know that $I_2 = h_f I_1 + h_o V_2$

$$\Rightarrow \frac{I_2}{V_2} = h_f \frac{I_1}{V_2} + h_o$$

$$\Rightarrow Y_o = h_f \frac{I_1}{V_2} + h_o \longrightarrow (1)$$

with $V_s = 0$, applying KVL in the input circuit of hybrid model

$$I_1 R_s + I_1 h_i + h_r V_2 = 0$$

$$I_1 (R_s + h_i) = -h_r V_2$$

$$\Rightarrow \frac{I_1}{V_2} = \frac{-h_r}{R_s + h_i} \longrightarrow (2)$$

substituting equation (2) in equation (1) we get

$$Y_o = h_f \left(\frac{-h_r}{R_s + h_i}\right) + h_o$$

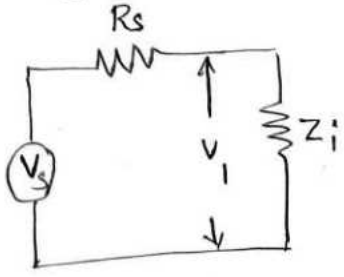
$$\Rightarrow \boxed{Y_o = h_o - \frac{h_f h_r}{R_s + h_i}}$$

and output impedance $Z_o = \frac{1}{Y_o} = \frac{1}{h_o - \frac{h_f h_r}{R_s + h_i}}$

Voltage Gain with source : (A_{VS})

Voltage Gain with source $(A_{VS}) = \frac{V_2}{V_s} = \frac{V_2}{V_1} \cdot \frac{V_1}{V_s}$

$$\Rightarrow A_{VS} = A_V \cdot \frac{V_1}{V_s} \longrightarrow (3)$$



from the figure $V_1 = \frac{V_s Z_i}{R_s + Z_i}$

$$\Rightarrow \frac{V_1}{V_s} = \frac{Z_i}{R_s + Z_i} \rightarrow (4)$$

substituting equation (4) in equation (3) we get

$$\boxed{A_{VS} = \frac{A_V \cdot Z_i}{R_s + Z_i}}$$

$$A_{VS} = \frac{\left(\frac{A_I R_L}{Z_i}\right) \cdot Z_i}{R_S + Z_i}$$

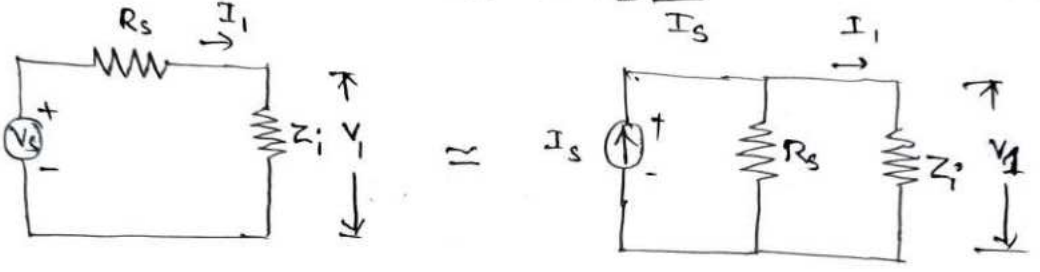
$$\therefore \boxed{A_{VS} = \frac{A_I R_L}{R_S + Z_i}}$$

Current Gain with source (A_{IS}):

Current Gain with source $(A_{IS}) = \frac{I_L}{I_S} = \frac{-I_2}{I_S}$

$$\Rightarrow A_{IS} = \frac{-I_2}{I_1} \cdot \frac{I_1}{I_S}$$

$$\Rightarrow A_{IS} = A_I \frac{I_1}{I_S} \longrightarrow (5)$$



From the above figure $I_1 = \frac{I_S \cdot R_S}{R_S + Z_i} \Rightarrow \frac{I_1}{I_S} = \frac{R_S}{R_S + Z_i} \longrightarrow (6)$

substituting equation (6) in equation (5) we get

$$\boxed{A_{IS} = \frac{A_I R_S}{R_S + Z_i}}$$

Power Gain: (A_P)

Power Gain $(A_P) = A_V \cdot A_I = \frac{A_I R_L}{Z_i} \cdot A_I$

$$\therefore \boxed{\text{Power Gain } (A_P) = \frac{A_I^2 R_L}{Z_i}}$$

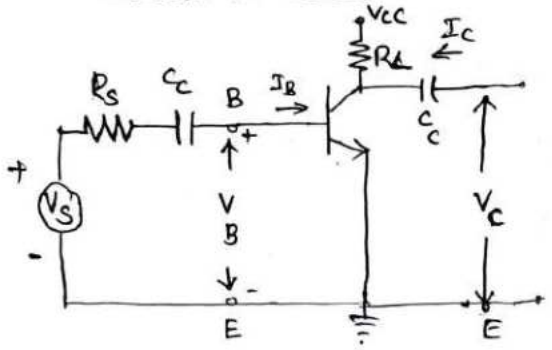
1) $A_I = \frac{-h_f}{1 + h_o R_L}$ 2) $Z_i = h_i + h_r A_I R_L = h_i - \frac{h_r h_f R_L}{1 + h_o R_L}$

3) $A_V = \frac{A_I R_L}{Z_i}$ 4) $Y_o = h_o - \frac{h_r h_f}{R_S + h_i}$ 5) $A_{IS} = \frac{A_I R_S}{R_S + Z_i}$

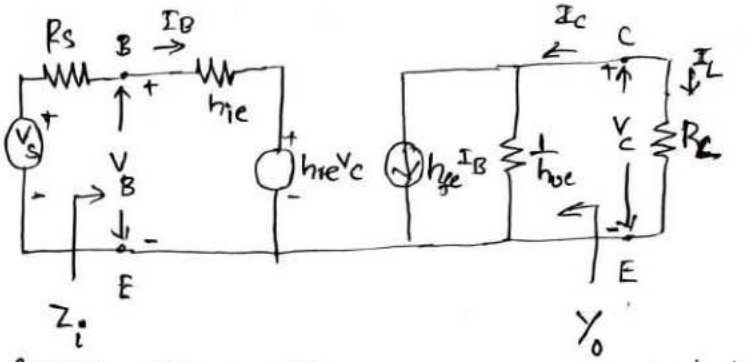
6) $A_{VS} = \frac{A_V Z_i}{R_S + Z_i} = \frac{A_I R_L}{R_S + Z_i}$ 7) $A_P = \frac{A_I^2 R_L}{Z_i}$

Small signal analysis of a Common Emitter Amplifier using exact h-Parameter model:

The Common Emitter Amplifier and it's equivalent h-parameter model are shown in below.



fig(a) CE amplifier



fig(b): CE amplifier h-parameter equivalent model. (Exact model)

To analyse the CE amplifier using h-parameter model, the following parameters are to be derived.

Current Gain (A_I):

Current Gain $A_I = \frac{I_L}{I_B} = \frac{-I_C}{I_B}$

we know that $I_C = h_{fe} I_B + h_{oe} V_c$ $\left(\because V_c = -I_C R_L \text{ From fig}\right)$

$$I_C = h_{fe} I_B + h_{oe}(-I_C R_L)$$

$$\Rightarrow I_C (1 + h_{oe} R_L) = h_{fe} I_B$$

$$\Rightarrow \frac{I_C}{I_B} = \frac{h_{fe}}{1 + h_{oe} R_L}$$

$$\therefore \boxed{A_I = \frac{-h_{fe}}{1 + h_{oe} R_L}}$$

Input impedance: (Z_i)

Input Impedance $(Z_i) = \frac{V_B}{I_B}$

we know that $V_B = h_{ie} I_B + h_{re} V_c$

$$V_B = h_{ie} I_B + h_{re}(-I_C R_L)$$

$$V_B = h_{ie} I_B + h_{re}(A_I I_B) R_L \quad \left(\because \frac{-I_c}{I_B} = A_I\right)$$

$$\therefore \quad V_B = I_B (h_{ie} + h_{re} A_I R_L)$$

$$\Rightarrow \quad \frac{V_B}{I_B} = h_{ie} + h_{re} A_I R_L$$

$$\therefore \quad \boxed{Z_i = h_{ie} + h_{re} A_I R_L}$$

$$\boxed{Z_i = h_{ie} - \frac{h_{re} h_{fe} R_L}{1 + h_{oe} R_L}} \qquad \left(\because A_I = \frac{-h_{fe}}{1 + h_{oe} R_L}\right)$$

Voltage Gain (A_v):

$$\text{Voltage Gain } (A_v) = \frac{V_c}{V_B} = \frac{-I_c R_L}{V_B} \qquad \left(\because \frac{-I_c}{I_B} = A_I\right)$$

$$\Rightarrow \quad A_v = \frac{A_I I_B R_L}{V_B}$$

$$\Rightarrow \quad \boxed{A_v = \frac{A_I R_L}{Z_i}} \qquad \left(\because \frac{V_B}{I_B} = Z_i\right)$$

output Admittance (Y_o):

$$\text{output admittance } (Y_o) = \frac{I_c}{V_c} = \frac{h_{fe} I_B + h_{oe} V_c}{V_c} \qquad \text{with } V_s = 0$$

$$\Rightarrow \quad Y_o = h_{fe} \frac{I_B}{V_c} + h_{oe} \longrightarrow (1)$$

when $V_s = 0$, applying KVL in the input circuit we get

$$I_B R_s + I_B h_{ie} + h_{re} V_c = 0$$

$$\Rightarrow \quad I_B (R_s + h_{ie}) = -h_{re} V_c$$

$$\Rightarrow \quad \frac{I_B}{V_c} = \frac{-h_{re}}{R_s + h_{ie}} \longrightarrow (2)$$

Substituting equation (2) in equation (1) we get

$$Y_o = h_{fe} \left(\frac{-h_{re}}{R_s + h_{ie}}\right) + h_{oe}$$

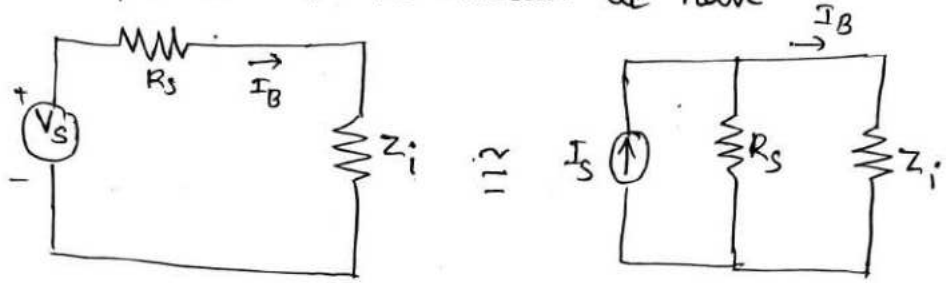
$$\therefore \quad \boxed{Y_o = h_{oe} - \frac{h_{re} h_{fe}}{R_s + h_{ie}}}$$

Current Gain with source (A_{IS}):

Current Gain with source $(A_{IS}) = \frac{-I_C}{I_S} = \frac{-I_C}{I_B} \cdot \frac{I_B}{I_S}$

$$\Rightarrow A_{IS} = A_I \cdot \frac{I_B}{I_S} \longrightarrow (3)$$

From the input side of the circuit we have



From the above figure $I_B = \frac{I_S R_S}{R_S + Z_i}$

$$\Rightarrow \frac{I_B}{I_S} = \frac{R_S}{R_S + Z_i} \longrightarrow (4)$$

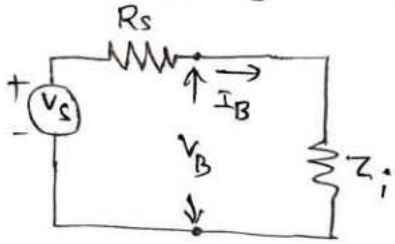
substituting equation (4) in equation (3) we get

$$\boxed{A_{IS} = \frac{A_I R_S}{R_S + Z_i}}$$

Voltage Gain with source (A_{VS}):

Voltage Gain with source $(A_{VS}) = \frac{V_C}{V_S} = \frac{V_C}{V_B} \cdot \frac{V_B}{V_S} = A_V \cdot \frac{V_B}{V_S} \rightarrow (5)$

From the figure $V_B = \frac{V_S Z_i}{R_S + Z_i}$



$$\therefore \frac{V_B}{V_S} = \frac{Z_i}{R_S + Z_i} \longrightarrow (6)$$

substituting equation (6) in equation (5) we get

$$\boxed{A_{VS} = \frac{A_V Z_i}{R_S + Z_i}} \longrightarrow (7)$$

we know that $A_V = \frac{A_I R_L}{Z_i}$ substituting this in eq (7) we get

$$\boxed{A_{VS} = \frac{A_I R_L}{R_S + Z_i}} \longrightarrow (8)$$

Equation (8) $\Rightarrow$ $A_{VS} = \dfrac{A_I R_L}{R_S + Z_i}$

$$A_{VS} = \frac{A_I R_S}{R_S + Z_i} \frac{R_L}{R_S}$$

$$\therefore \boxed{A_{VS} = \frac{A_{IS} R_L}{R_S}}$$

Power Gain (A_p) :

Power Gain (A_p) = Voltage Gain (A_V) $\times$ Current Gain (A_I)

$$= A_V \cdot A_I$$

$$A_p = \frac{A_I R_L}{Z_i} A_I$$

$$\therefore \boxed{A_p = \frac{A_I^2 R_L}{Z_i}}$$

1) current Gain (A_I) = $\dfrac{-h_{fe}}{1 + h_{oe} R_L}$

2) Input Impedance (Z_i) = $h_{ie} + h_{re} A_I R_L$

and $Z_i = h_{ie} - \dfrac{h_{re} h_{fe}}{1 + h_{oe} R_L} R_L$

3) Voltage Gain (A_V) = $\dfrac{A_I R_L}{Z_i}$

4) output admittance $Y_o = h_{oe} - \dfrac{h_{re} h_{fe}}{R_S + h_{ie}}$

and output impedance (Z_o) = $\dfrac{1}{h_{oe} - \dfrac{h_{re} h_{fe}}{R_S + h_{ie}}}$

5) current Gain with source (A_{IS}) = $\dfrac{A_I R_S}{R_S + Z_i}$

6) Voltage Gain with source (A_{VS}) = $\dfrac{A_V Z_i}{R_S + Z_i}$

(or) $A_{VS} = \dfrac{A_I R_L}{R_S + Z_i} = \dfrac{A_{IS} R_L}{R_S}$

7) Power Gain $A_p = \dfrac{A_I^2 R_L}{Z_i}$

Analysis of a common collector amplifier (Emitter follower) using exact h-parameter model :

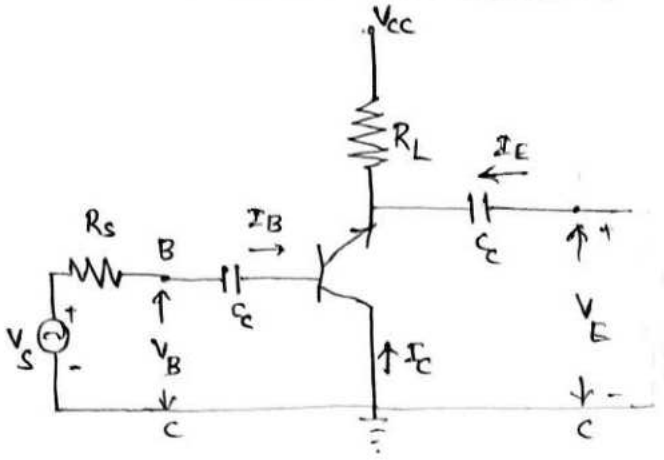
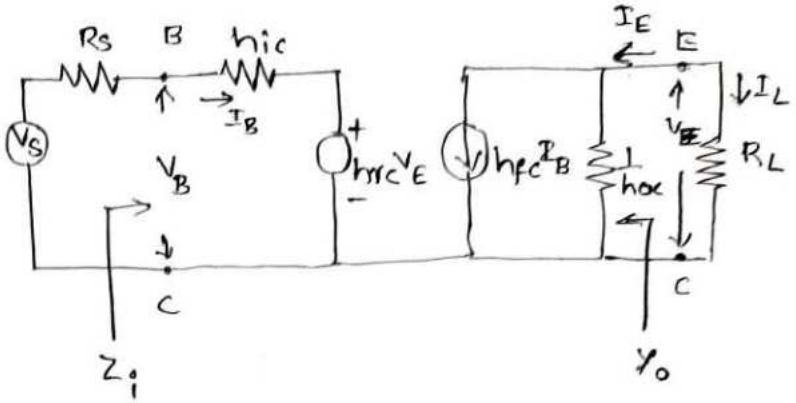


fig: (a) common collector Amplifier



fig(b): Exact h-parameter model of a common collector amplifier.

To analyse the common collector amplifier using h-parameter model, the following parameters are to be derived.

Current Gain (A_I) :

$$\text{Current Gain } (A_I) = \frac{I_L}{I_B} = \frac{-I_E}{I_B}$$

we know that $I_E = h_{fc} I_B + h_{oc} V_E$

$$I_E = h_{fc} I_B + h_{oc}(-I_E R_L)$$

$$\Rightarrow I_E(1 + h_{oc} R_L) = h_{fc} I_B$$

$$\therefore \frac{I_E}{I_B} = \frac{h_{fc}}{1 + h_{oc} R_L}$$

but $A_I = \frac{-I_E}{I_B}$ so $\boxed{A_I = \frac{-h_{fc}}{1 + h_{oc} R_L}}$

Input impedance (Z_i) :

$$\text{Input impedance } (Z_i) = \frac{V_B}{I_B}$$

we know that $V_B = h_{ic} I_B + h_{rc} V_E$

$$\Rightarrow V_B = h_{ic} I_B + h_{rc}(-I_E R_L)$$

$$\Rightarrow V_B = h_{ic} I_B + h_{rc}(A_I I_B) R_L \quad \left(\because A_I = \frac{-I_E}{I_B}\right)$$

$$\Rightarrow \quad \frac{V_B}{I_B} = h_{ic} + h_{rc} A_I R_L$$

$$\therefore \boxed{Z_i = h_{ic} + h_{rc} A_I R_L}$$

substituting $A_I = \frac{-h_{fc}}{1 + h_{oc} R_L}$ in the above equation, we get

$$\boxed{Z_i = h_{ic} - \frac{h_{rc} h_{fc} R_L}{1 + h_{oc} R_L}}$$

Voltage Gain (A_V):

$$\text{Voltage Gain } (A_V) = \frac{V_E}{V_B} = \frac{-I_E R_L}{V_B}$$

$$\Rightarrow \quad A_V = \frac{(A_I I_B) R_L}{V_B} \qquad \left(\because A_I = \frac{-I_E}{I_B}\right)$$

$$\Rightarrow \quad \boxed{A_V = \frac{A_I R_L}{Z_i}} \qquad \left(\because Z_i = \frac{V_B}{I_B}\right)$$

output Admittance (Y_o):

output admittance $Y_o = \frac{I_E}{V_E}$ with $V_s = 0$.

we know that $I_E = h_{fc} I_B + h_{oc} V_E$

$$\therefore \quad Y_o = \frac{h_{fc} I_B + h_{oc} V_E}{V_E}$$

$$Y_o = h_{fc}\left(\frac{I_B}{V_E}\right) + h_{oc} \longrightarrow (1)$$

From fig(b) when $V_s = 0$ we can write

$$I_B R_s + \frac{I}{B} \cdot h_{ic} + h_{rc} V_E = 0$$

$$\Rightarrow \quad I_B (R_s + h_{ic}) = -h_{rc} V_E$$

$$\therefore \quad \frac{I_B}{V_E} = -\frac{h_{rc}}{R_s + h_{ic}} \longrightarrow (2)$$

Substituting eq(2) in eq(1)

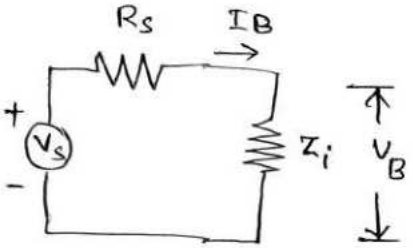
we get $$Y_o = h_{oc} - \frac{h_{fc}\, h_{rc}}{R_s + h_{ic}}$$

The output Impedance $$Z_o = \frac{1}{Y_o} = \frac{1}{h_{oc} - \frac{h_{fc}\, h_{rc}}{R_s + h_{ic}}}$$

Current Gain with source (A_{IS}):

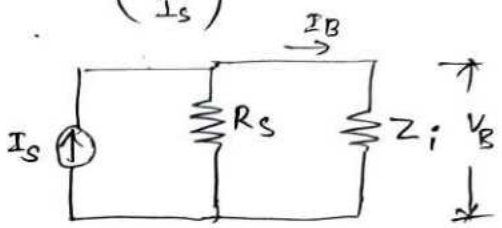
Current gain with source $(A_{IS}) = \frac{-I_E}{I_S} = \frac{-I_E}{I_B} \cdot \frac{I_B}{I_S}$

$$\Rightarrow A_{IS} = A_I \cdot \left(\frac{I_B}{I_S}\right) \longrightarrow (3)$$



Input section of hybrid model

$\equiv$



Input section of hybrid model with Current source instead of voltage source

From the figure $$I_B = \frac{I_S R_S}{R_S + Z_i}$$

$$\Rightarrow \frac{I_B}{I_S} = \frac{R_S}{R_S + Z_i} \longrightarrow (4)$$

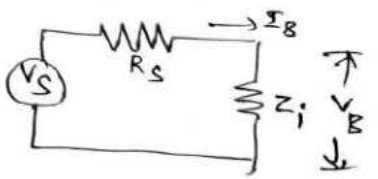
Substituting equation (4) in eq(3) we get

$$A_{IS} = \frac{A_I R_S}{R_S + Z_i}$$

Voltage Gain with source (A_{VS}):

Voltage Gain with source $A_{VS} = \frac{V_E}{V_S} = \frac{V_E}{V_B} \cdot \frac{V_B}{V_S}$

$$\Rightarrow A_{VS} = A_V \cdot \frac{V_B}{V_S} \longrightarrow (5)$$



from the figure $$V_B = \frac{V_S \cdot Z_i}{R_S + Z_i}$$

$$\Rightarrow \frac{V_B}{V_S} = \frac{Z_i}{R_S + Z_i} \longrightarrow (6)$$

Substituting equation (6) in (5) we get

$$\boxed{A_{VS} = \frac{A_V Z_i}{R_S + Z_i}}$$

substituting $A_V = \frac{A_I R_L}{Z_i}$ in the above equation we get

$$\boxed{A_{VS} = \frac{A_I R_L}{R_S + Z_i}}$$

$$\Rightarrow \quad A_{VS} = \left(\frac{A_I R_S}{R_S + Z_i}\right) \frac{R_L}{R_S}$$

$$\boxed{A_{VS} = \frac{A_{IS} R_L}{R_S}}$$

Power Gain (A_P):

Power Gain (A_P) = Voltagain x Current Gain

$$= A_V \cdot A_I$$

$$= \left(\frac{A_I R_L}{Z_i}\right) A_I$$

$$\therefore \quad \boxed{A_P = \frac{A_I^2 R_L}{Z_i}}$$

1) Current Gain $A_I = \frac{-h_{fc}}{1 + h_{oc} R_L}$

2) Input impedance $Z_i = h_{ic} + h_{rc} A_I R_L$

$$Z_i = h_{ic} - \frac{h_{rc} h_{fc} R_L}{1 + h_{oc} R_L}$$

3) voltage Gain $A_V = \frac{A_I R_L}{Z_i}$

4) output admittance $Y_o = h_{oc} - \frac{h_{rc} h_{fc}}{R_S + h_{ic}}$

output impedance $Z_o = \frac{1}{Y_o} = \frac{1}{h_{oc} - \frac{h_{rc} h_{fc}}{R_S + h_{ic}}}$

5) voltage with source (A_{VS})

$$A_{VS} = \frac{A_V Z_i}{R_S + Z_i}$$

(or) $$A_{VS} = \frac{A_I R_L}{R_S + Z_i}$$

(or) $$A_{VS} = \frac{A_{IS} \cdot R_L}{R_S}$$

6) Current gain with source

$$A_{IS} = \frac{A_I R_S}{R_S + Z_i}$$

7) Power Gain (A_P) = $\frac{A_I^2 R_L}{Z_i}$

Exact Analysis of a Common base amplifier using h-parameter model:

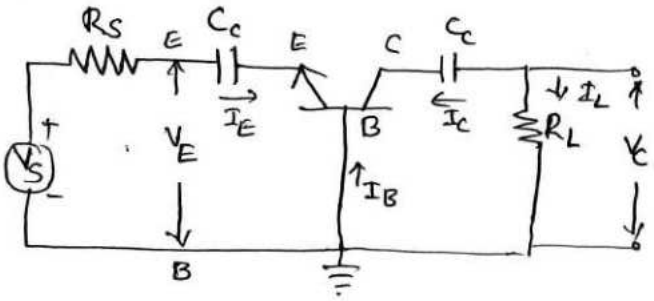


fig a) CB amplifier

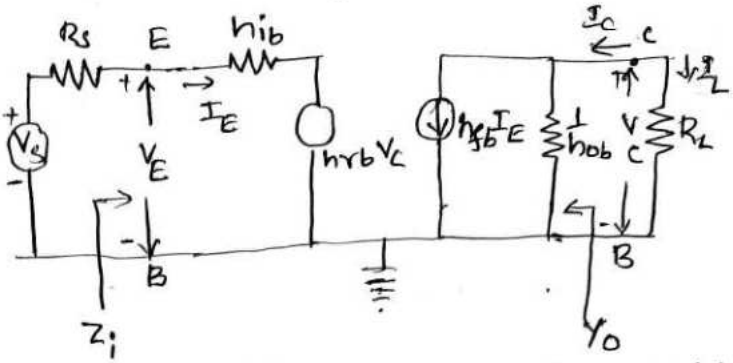


fig b) CB amplifier h-parameter model.

To analyse CB amplifier the following parameters are to be derived.

1) Current Gain (A_I):

$$\text{Current gain } (A_I) = \frac{I_L}{I_E} = \frac{-I_C}{I_E}$$

we know that $I_C = h_{fb} I_E + h_{ob} V_C$

$$I_C = h_{fb} I_E + h_{ob}(-I_C R_L)$$

$$I_C (1 + h_{ob} R_L) = h_{fb} I_E$$

$$\frac{I_C}{I_E} = \frac{h_{fb}}{1 + h_{ob} R_L}$$

but $A_I = -\frac{I_C}{I_E}$ so $\boxed{A_I = -\frac{h_{fb}}{1 + h_{ob} R_L}}$

2) Input Impedance (Z_i):

$$\text{Input impedance } (Z_i) = \frac{V_E}{I_E}$$

we know that $V_E = h_{ib} I_E + h_{rb} V_C$

$$V_E = h_{ib} I_E + h_{rb}(-I_C R_L) \qquad \left(\because \frac{-I_C}{I_E} = A_I\right)$$

$$V_E = h_{ib} I_E + h_{rb} A_I I_E R_L$$

$$\Rightarrow \frac{V_E}{I_E} = h_{ib} + h_{rb} A_I R_L$$

$$\therefore \boxed{Z_i = h_{ib} + h_{rb} A_I R_L}$$

Substituting $A_I = \frac{-h_{fb}}{1+h_{ob}R_L}$ in the above equation we get

$$\boxed{Z_i = h_{ib} - \frac{h_{rb}h_{fb}.R_L}{1+h_{ob}R_L}}$$

3) Voltage Gain (A_V): Voltage Gain $A_V = \frac{V_C}{V_E}$

$$A_V = \frac{-I_C R_L}{V_E}$$

$$= \frac{(A_I I_E)R_L}{V_E} \quad \left(\because A_I = -\frac{I_C}{I_E}\right)$$

$$\therefore \boxed{A_V = \frac{A_I R_L}{Z_i}} \quad \left(\because Z_i = \frac{V_E}{I_E}\right)$$

4) output admittance (Y_o):

output admittance $Y_o = \frac{I_C}{V_C}$ with $R_s = 0$

$$= \frac{h_{fb}I_E + h_{ob}V_C}{V_C}$$

$$Y_o = h_{ob} + h_{fb}\left(\frac{I_E}{V_C}\right) \longrightarrow (1)$$

when $V_s = 0$, Applying KVL to the input circuit we get

$$I_E R_s + I_E h_{ib} + h_{rb}V_C = 0$$

$$\Rightarrow \frac{I_E}{V_C} = \frac{-h_{rb}}{R_s + h_{ib}} \longrightarrow (2)$$

Substituting eq(2) in eq(1) we get

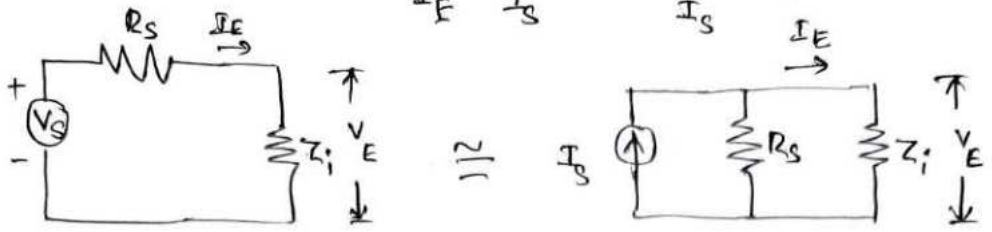
$$\boxed{Y_o = h_{ob} - \frac{h_{fb}h_{rb}}{R_s + h_{ib}}}$$

output impedance $Z_o = \frac{1}{Y_o} = \frac{1}{h_{ob} - \frac{h_{fb}h_{rb}}{R_s+h_{ib}}}$

5) Current Gain with source (A_{IS}):

Current Gain with source $A_{IS} = \frac{I_L}{I_S} = -\frac{I_C}{I_S}$

$$\Rightarrow A_{IS} = -\frac{I_C}{I_E}\frac{I_E}{I_S} = A_I \cdot \frac{I_E}{I_S} \longrightarrow (3)$$



From the above figure $I_E = \frac{I_S R_s}{R_s + Z_i}$

$$\Rightarrow \frac{I_E}{I_S} = \frac{R_s}{R_s + Z_i} \longrightarrow (4)$$

substituting eq (4) in eq (3) we get

$$\boxed{A_{IS} = \frac{A_I R_s}{R_s + Z_i}}$$

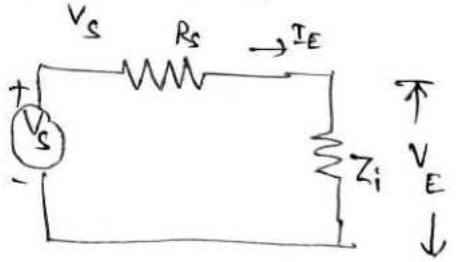
6) Voltage Gain with Source (A_{VS}):

Voltage Gain with source $(A_{VS}) = \frac{V_C}{V_S} = \frac{V_C}{V_E}\cdot\frac{V_E}{V_S}$

$$\Rightarrow A_{VS} = A_V \cdot \frac{V_E}{V_S} \longrightarrow (5)$$

From the figure

$$V_E = \frac{V_S Z_i}{R_s + Z_i} \longrightarrow (6)$$



Substi $\frac{V_E}{V_S} = \frac{Z_i}{R_s + Z_i}$ in eq (5) we get

$$\boxed{A_{VS} = \frac{A_V Z_i}{R_s + Z_i}}$$

Substituting $A_V = \frac{A_I R_L}{Z_i}$ in the above eq we get $\boxed{A_{VS} = \frac{A_I R_L}{R_s + Z_i}}$

$$\Rightarrow \quad A_{VS} = \frac{A_I R_S}{R_S + Z_i} \frac{R_L}{R_S}$$

$$\therefore \boxed{A_{VS} = \frac{A_{IS} R_L}{R_S}}$$

7) **Power Gain (A_P):** Power Gain $(A_P) = A_V \cdot A_I$

$$= \frac{A_I R_L}{Z_i} A_I$$

$$\therefore \boxed{A_P = \frac{A_I^2 R_L}{Z_i}}$$

---

1) Current Gain $A_I = \frac{-h_{fb}}{1 + h_{ob} R_L}$

2) Input Impedance $Z_i = h_{ib} + h_{rb} A_I R_L$

$$Z_i = h_{ib} - \frac{h_{rb} h_{fb} R_L}{1 + h_{ob} R_L}$$

3) Voltage Gain $A_V = \frac{A_I R_L}{Z_i}$

4) Output Admittance $Y_o = h_{ob} - \frac{h_{rb} h_{fb}}{R_S + h_{ib}}$

Output Impedance $Z_o = \frac{1}{Y_o} = \frac{1}{h_{ob} - \frac{h_{rb} h_{fb}}{R_S + h_{ib}}}$

5) Current Gain with source $(A_{IS}) = \frac{A_I R_S}{R_S + Z_i}$

6) Voltage Gain with source $(A_{VS}) = \frac{A_V Z_i}{R_S + Z_i}$

(or) $A_{VS} = \frac{A_I R_L}{R_S + Z_i}$

(or) $A_{VS} = \frac{A_{IS} R_L}{R_S}$

7) Power Gain $(A_P) = \frac{A_I^2 R_L}{Z_i}$

Approximate (or) Simplified h-parameter model for a transistor amplifier:

In most of the practical cases it may be required to obtain the approximate values of current gain, input impedance, voltage gain, output admittance etc rather than their exact values which require lengthy calculations.

But All the times we cannot go for simplified h-parameter model. Since common Emitter is most widely used amplifier, it is taken into consideration. The exact model for CE amplifier using h-parameters is as shown in below.

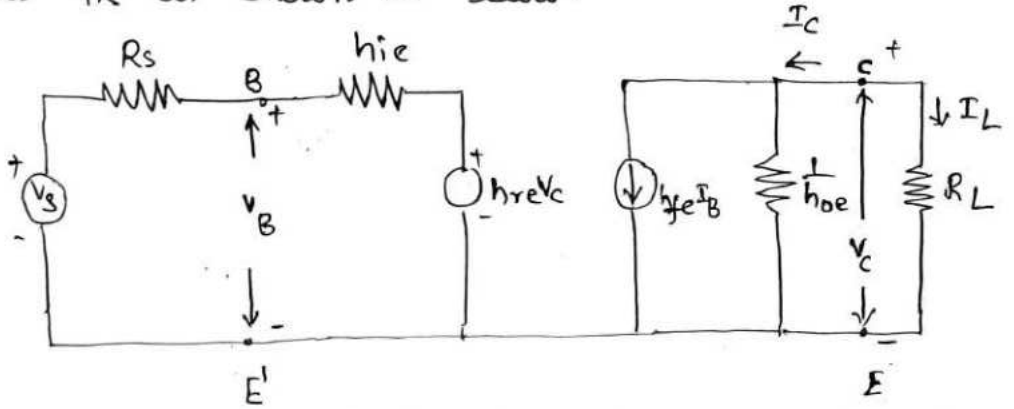


fig: Exact h-parameter model for CE amplifier

Here $\frac{1}{h_{oe}}$ is in parallel with R_L. The parallel combination of two unequal impedances i.e $\frac{1}{h_{oe}}$ and R_L is approximately equal to Lower value i.e R_L. Hence if $\frac{1}{h_{oe}} >> R_L$, then h_{oe} may be neglected provided $h_{oe}R_L < 0.1$.

If h_{oe} is neglected, Collector current I_C becomes $I_C = h_{fe}I_B$

under this condition $h_{re}|V_C| \simeq h_{re}I_C R_L = h_{re}h_{fe}I_B R_L$

Since $h_{re}\cdot h_{fe} \simeq 0.01$, $h_{re}V_C$ can be neglected, provided R_L is not too large.

As a conclusion, if R_L is small it is possible to neglect the parameters h_{re} and h_{oe} and we can obtain the approximate h-parameter model.

It can be shown that if $h_{oe}R_L \leq 0.1$ the error in calculating A_I, A_V, Z_i and Y_o for CE configuration is less than 10%.

Analysis of CE configuration using approximate h-parameter model: The approximate hybrid model for CE configuration is as shown in below.

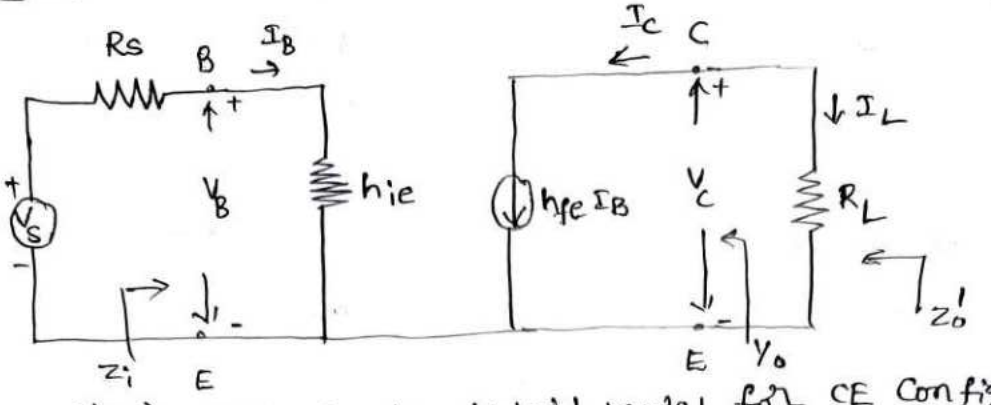


fig a) Approximate hybrid model for CE Configuration

The approximate hybrid model, which is valid for all types of Configurations of a transistor is shown in figure (b).

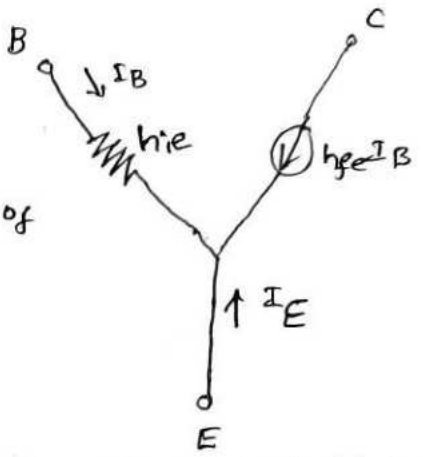


fig b): Approximate hybrid model Valid for all configurations.

The parameters for an approximated hybrid model of CE are derived below.

Current Gain (A_I):

The Current Gain (A_I) for CE configuration using exact h-parameter model is

$$\text{Current Gain } (A_I) = -\frac{h_{fe}}{1 + h_{oe} R_L}$$

If $h_{oe} R_L < 0.1$, $A_I = -h_{fe}$

$$\therefore \boxed{\text{Current Gain } (A_I) \simeq -h_{fe}}$$

Input Impedance (Z_i):

The input impedance (Z_i) for Common Emitter using exact h-parameter model is

$$Z_i = h_{ie} + h_{re} \cdot A_I R_L$$

$$Z_i = h_{ie} + h_{re} \cdot (-h_{fe}) R_L$$

$$= h_{ie} - (h_{re} \cdot h_{fe} R_L)$$

since $h_{re} \cdot h_{fe} \simeq 0.01$ if R_L value is not too large we can -

neglect $h_{re} \cdot h_{fe} \cdot R_L$.

$\therefore$ **Input impedance $z_i \simeq h_{ie}$**

Voltage Gain (A_v):

we know that the voltage gain $(A_v) = \frac{A_I R_L}{z_i}$

$\Rightarrow$ **$A_v = -\frac{h_{fe} R_L}{h_{ie}}$**

output admittance: (Y_o)

we know that the output admittance $(Y_o) = h_{oe} - \frac{h_{fe} h_{re}}{R_s + h_{ie}}$

Neglecting h_{oe}, h_{re} we get $Y_o = 0$

$\therefore$ output admittance **$Y_o = 0$**

The output Impedance $Z_o = \frac{1}{Y_o} = \frac{1}{0} = \infty$.

$\therefore$ **$Z_o = \infty$**

$z_o' = z_o \| R_L \simeq R_L$ where z_o' = o/p impedance along with R_L

Analysis of CC configuration using approximate h-parameter model:

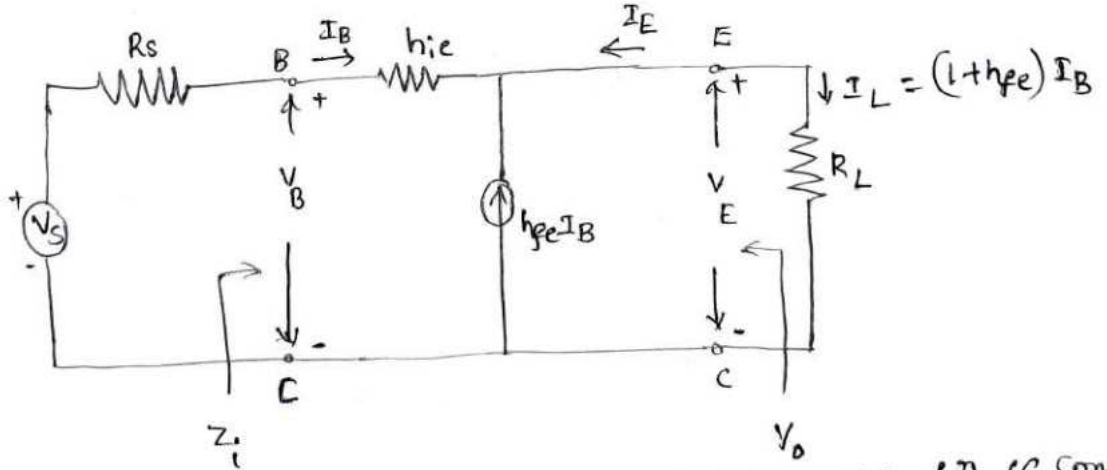


fig: simplified (a) approximated hybrid model for CC configuration

The above figure shows the approximated hybrid model for CC amplifier using which we derive the following parameters such as current-gain (A_I), voltage Gain (A_v), Input impedance (z_i) and output admittance (Y_o) etc. Common Collector amplifier is also known as Emitter follower.

Current Gain (A_I):

$$\text{Current Gain } (A_I) = \frac{I_L}{I_B} = \frac{(1+h_{fe})I_B}{I_B} = 1+h_{fe}$$

$$\therefore \quad \boxed{A_I = 1+h_{fe}}$$

(∵ From figure $I_L = (1+h_{fe})I_B$)

Input impedance (Z_i):

From the figure $Z_i = \frac{V_B}{I_B}$

Applying KVL we have (at the input side of the circuit)

$$V_B = I_B h_{ie} + I_L R_L$$

$$V_B = I_B h_{ie} + (1+h_{fe}) I_B R_L$$

$$\Rightarrow \quad \frac{V_B}{I_B} = h_{ie} + (1+h_{fe}) R_L$$

$$\therefore \quad \boxed{Z_i = h_{ie} + (1+h_{fe}) R_L}$$

From this equation the input impedance of CC amplifier is clearly observed to be greater than that of CE amplifier.

Voltage Gain (A_V):

$$\text{The voltage Gain } (A_V) = \frac{V_E}{V_B} = \frac{I_L R_L}{h_{ie} I_B + I_L R_L}$$

$$\Rightarrow \quad A_V = \frac{(1+h_{fe}) I_B \cdot R_L}{h_{ie} I_B + (1+h_{fe}) I_B R_L}$$

$$\Rightarrow \quad \boxed{A_V = \frac{(1+h_{fe}) R_L}{h_{ie} + (1+h_{fe}) R_L}}$$

we know that $(1+h_{fe})R_L >> h_{ie}$ neglecting h_{ie} in the denominator we get

$$A_V \simeq \frac{(1+h_{fe})R_L}{(1+h_{fe})R_L} \simeq 1$$

$$\therefore \quad \boxed{A_V \simeq 1}$$

The output admittance (Y_o) :

The output admittance $Y_o = \frac{I_E}{V_E}$ with $V_s = 0$. $\longrightarrow$ (1)

Applying KVL to the above circuit assuming $V_s = 0$ we get

$$I_B R_s + I_B h_{ie} + V_E = 0$$

$$V_E = -I_B (R_s + h_{ie}) \longrightarrow (2)$$

From the figure $I_E = -I_L = -(1 + h_{fe}) I_B \longrightarrow (3)$

substituting eq (2) and eq (3) in eq (1) we get

$$Y_o = \frac{-(1+h_{fe})I_B}{-I_B(R_s + h_{ie})} = \frac{1+h_{fe}}{R_s + h_{ie}}$$

$$\therefore \boxed{Y_o = \frac{1 + h_{fe}}{R_s + h_{ie}}}$$

The output impedance $\boxed{Z_o = \frac{1}{Y_o} = \frac{R_s + h_{ie}}{1 + h_{fe}}}$

The output impedance along with $R_L = Z_o' = Z_o \| R_L$.

Analysis of common base configuration using approximate h-parameter model;

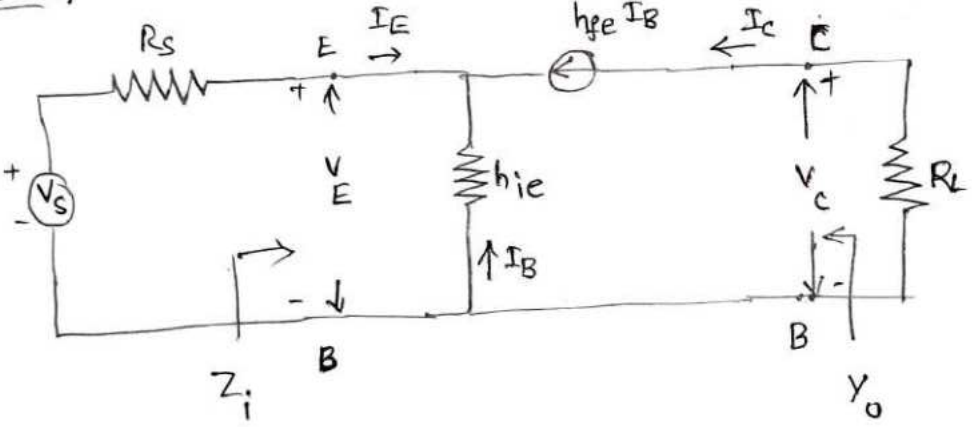


fig: Simplified hybrid model for common base amplifier.

To analyse the common base amplifier using approximate h-parameter model, we have to derive the parameters such as current gain (A_I), input impedance (Z_i), voltage gain (A_V) and output admittance (Y_o) etc.

Current Gain: (A_I)

$$\text{Current Gain } A_I = \frac{-I_C}{-I_E} = \frac{I_L}{I_E} \longrightarrow (1)$$

From the figure $I_C = h_{fe} I_B$ and $I_E = -(h_{fe} I_B + I_B)$

substituting these equations in equation (1) we get

$$A_I = \frac{-h_{fe} I_B}{-(h_{fe} I_B + I_B)}$$

$$\therefore \boxed{A_I = \frac{h_{fe}}{1+h_{fe}} = -h_{fb}}$$

Input impedance (Z_i):

$$\text{Input impedance } Z_i = \frac{V_E}{I_E} = \frac{-h_{ie} I_B}{-(I_B + h_{fe} I_B)}$$

$$\Rightarrow Z_i = \frac{h_{ie} I_B}{(1+h_{fe}) I_B} = \frac{h_{ie}}{1+h_{fe}}$$

$$\therefore \boxed{Z_i = \frac{h_{ie}}{1+h_{fe}} = h_{ib}}$$

Voltage Gain (A_V):

$$\text{Voltage Gain } A_V = \frac{V_C}{V_E} = \frac{-I_C R_L}{-h_{ie} I_B}$$

$$\Rightarrow A_V = \frac{-h_{fe} I_B R_L}{-h_{ie} I_B} = \frac{h_{fe} R_L}{h_{ie}}$$

$$\therefore \boxed{A_V = \frac{h_{fe} R_L}{h_{ie}}}$$

output admittance (Y_o):

$$Y_o = \frac{I_C}{V_C} \text{ with } V_s = 0$$

From the figure when $V_s = 0$, $I_b = 0$ and $I_E = 0$ and hence $I_c = 0$

$\therefore \boxed{Y_o = 0}$ Therefore $\boxed{\text{output Impedance } Z_o = \infty}$

o/p impedance along with R_L, $Z_o' = Z_o \| R_L = R_L$

NOTE: The typical values of h-parameters when the transistor is connected in CE Configuration are $h_{ie} = 1.1K\Omega$, $h_{fe} = 50$, $h_{re} = 2.5 \times 10^{-4}$ and $h_{oe} = 25\mu A/V$

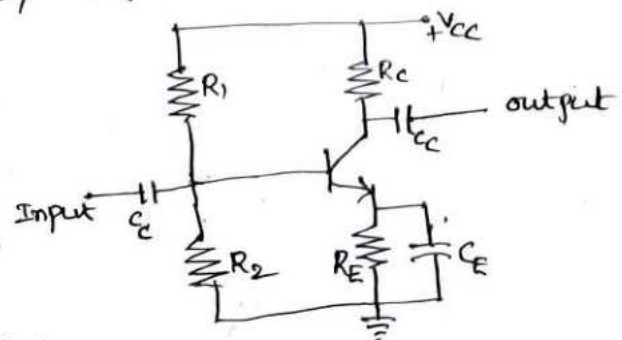
Conversion formulae for h-parameters

Common Collector	Common Base
1) $h_{ic} = h_{ie}$	1) $h_{ib} = \frac{h_{ie}}{1+h_{fe}}$
2) $h_{rc} = 1$	2) $h_{rb} = \frac{h_{ie} h_{oe}}{1+h_{fe}} - h_{re}$
3) $h_{fc} = -(1+h_{fe})$	3) $h_{fb} = \frac{-h_{fe}}{1+h_{fe}}$
4) $h_{oc} = h_{oe}$	4) $h_{ob} = \frac{h_{oe}}{1+h_{fe}}$

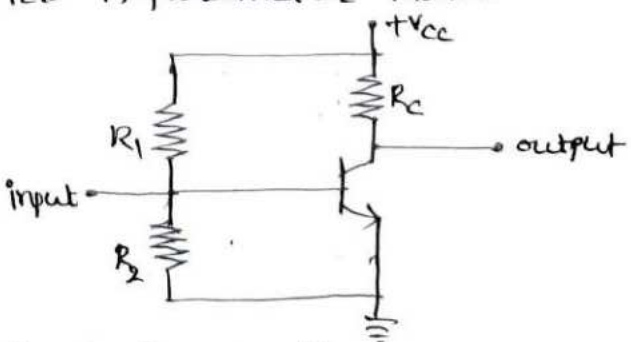
Guidelines for the analysis of a transistor amplifier:

There are different biasing techniques, different Configurations and so on. The analysis of such transistor circuits can be done by following the simple guidelines given below.

1) Draw the actual circuit diagram
2) Replace the coupling capacitors and emitter bypass capacitor by short circuit
3) Replace DC source by short circuit. In other words short V_{cc} and ground lines
4) Mark the points B (base), C (collector) and Emitter E on the Circuit diagram
5) Replace the transistor by it's h-parameter model.



fig(a) Actual circuit



fig(b): Circuit with capacitors as a short - Circuit

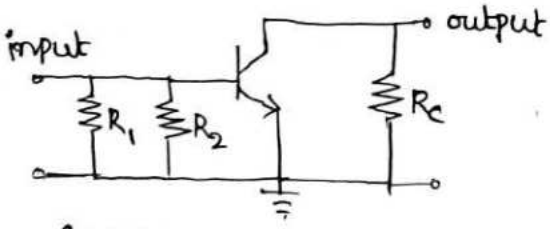


fig (c): Circuit with V_{cc} and Ground - Short Circuit.

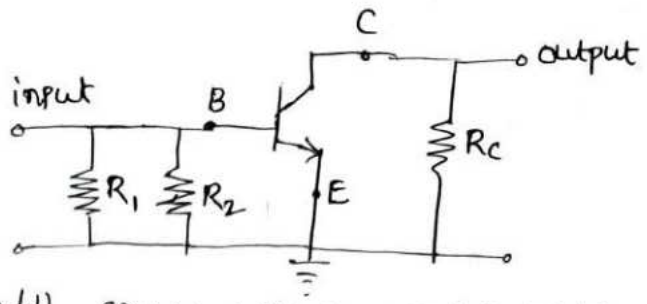


fig (d) Circuit with B, C, and E points located.

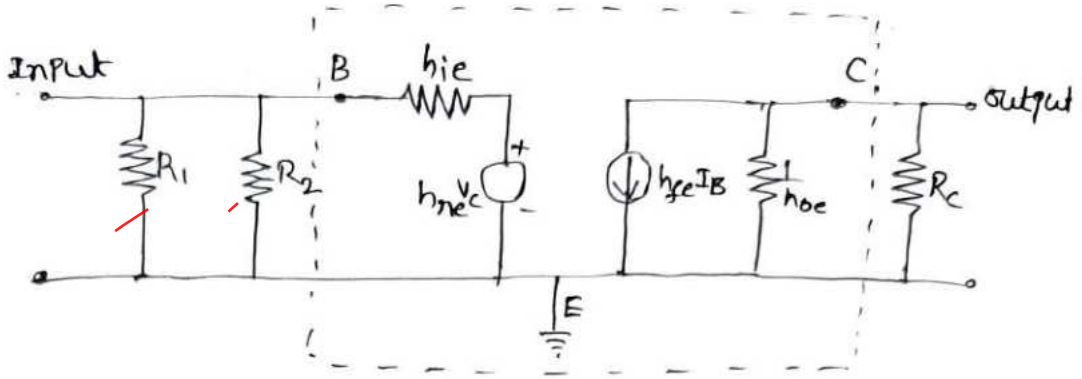
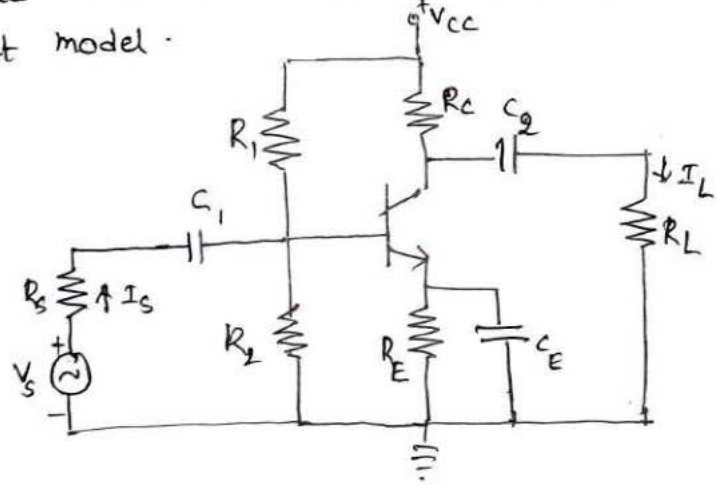


fig (e) Circuit with transistor replaced by h-parameter equivalent.

Problem: Consider a single stage CE amplifier with $R_s = 1k\Omega$, $R_1 = 50k\Omega$, $R_2 = 2k\Omega$, $R_c = 1k\Omega$, $R_L = 1.2k\Omega$, $h_{fe} = 50$, $h_{ie} = 1.1k\Omega$, $h_{oe} = 25\mu A/V$ and $h_{re} = 2.5 \times 10^{-4}$ as shown in below. Find $A_i, Z_i, A_V, Y_o, A_{IS}$ and A_{Vs}. Use Exact model.



NOTE: This circuit is a common emitter amplifier with Emitter bypass capacitor C_E in parallel with the Emitter resistance R_E

Sol)

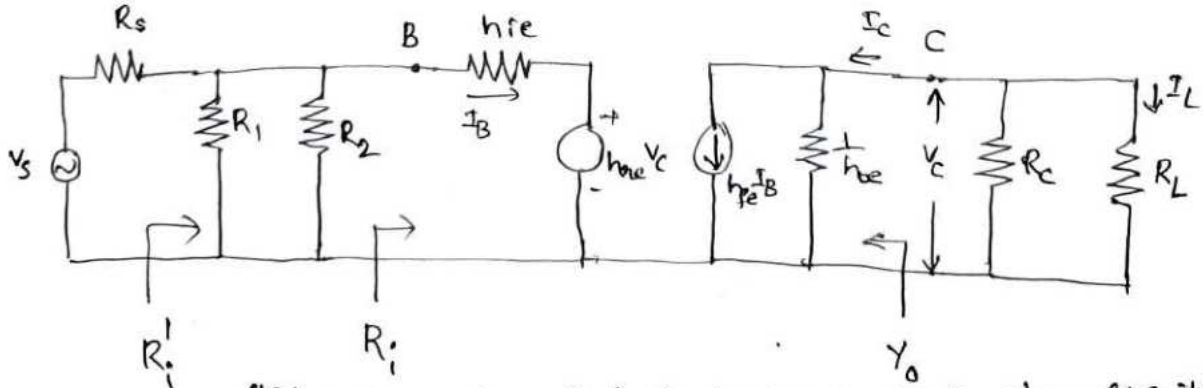


fig: H-Parameter equivalent circuit for the given circuit

Current Gain $(A_I) = \frac{-I_c}{I_B} = \frac{-h_{fe}}{1+h_{oe}R_L'}$

where $R_L' = R_c \| R_L = 1k\Omega \| 1.2k\Omega$

$R_L' = \frac{(1\times10^3)\times(1.2\times10^3)}{(1\times10^3)+(1.2\times10^3)} = \frac{1.2\times10^6}{2.2\times10^3} = 545.45\Omega$

$\therefore A_I = \frac{-50}{1+(25\times10^{-6}\times 545.45)} = -49.32$

Input Impedance $Z_i = h_{ie} + h_{re}A_I R_L'$

$= 1100 + (2.5\times10^{-4}\times(-49.32)\times 545.45)$

$\therefore Z_i = 1093.27\Omega$

Voltage Gain $A_V = \frac{A_I R_L'}{Z_i} = \frac{-49.32\times 545.45}{1093.27}$

$\therefore A_V = -24.606$

output admittance $Y_o = h_{oe} - \frac{h_{re}h_{fe}}{R_S'+h_{ie}}$

$\left(\because R_S' = R_S \| R_1 \| R_2 = 1k\Omega \| 50k\Omega \| 2k\Omega = 657.5\Omega\right)$

$= 25\times10^{-6} - \frac{2.5\times10^{-4}\times 50}{657.5+1100}$

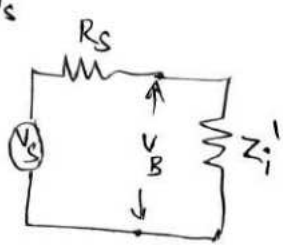
$= 25\times10^{-6} - 7.112\times10^{-6}$

$\therefore Y_o = 17.88\times10^{-6}\ \mho$

output Impedance $Z_o = \frac{1}{Y_o} = \frac{1}{17.88\times10^{-6}} = 55.9\ k\Omega$

Voltage Gain with source $A_{VS} = \frac{V_c}{V_S} = \frac{V_c}{V_B}\cdot\frac{V_B}{V_S}$

$\Rightarrow A_{VS} = A_V \cdot \frac{\left(\frac{V_S\cdot Z_i'}{Z_i'+R_S}\right)}{V_S}$



$\Rightarrow A_{VS} = \frac{A_V Z_i'}{Z_i'+R_S}$

where $Z_i' = Z_i \| R_1 \| R_2 = 1093.27 \| 50k\Omega \| 2k\Omega$

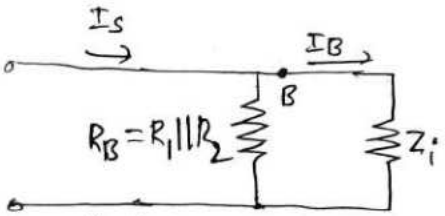
$= 1093.27 \| 1.92k\Omega$

$Z_i' = 696.61\ \Omega$

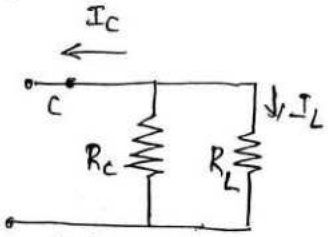
$\therefore A_{VS} = \frac{A_V Z_i'}{R_S + Z_i'} = \frac{-24.606 \times 696.61}{1000 + 696.61}$

$\therefore A_{VS} = -10.102$

Current Gain with source (A_{IS}) :



fig(a)



fig(b)

$A_{IS} = \frac{I_L'}{I_S} = \frac{I_L}{I_C} \cdot \frac{I_C}{I_B} \cdot \frac{I_B}{I_S}$ → eq (A)

$\Rightarrow A_{IS} = \frac{I_L}{I_C}(-A_I) \cdot \frac{I_B}{I_S}$ → (1)

From above fig(b) $I_L = \frac{-I_C \cdot R_C}{R_C + R_L} \Rightarrow \frac{I_L}{I_C} = -\frac{R_C}{R_C + R_L}$ → (2)

From fig(a) $I_B = \frac{I_S R_B}{R_B + Z_i} \Rightarrow \frac{I_B}{I_S} = \frac{R_B}{R_B + Z_i}$ → (3)

where $R_B = R_1 \| R_2 = 50k\Omega \| 2k\Omega = 1.923k\Omega$

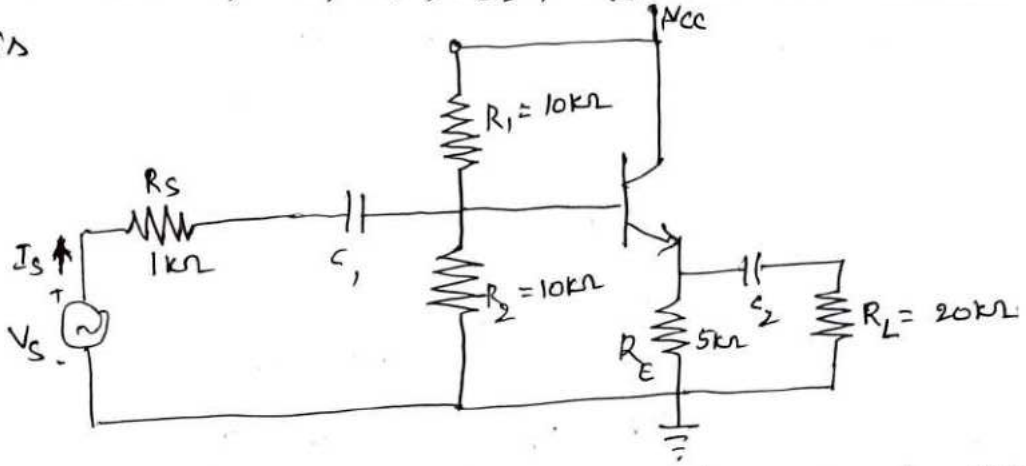
Substituting eq (3), eq (2) together in eq (1) we get

$A_{IS} = \frac{-R_C}{R_C + R_L} \cdot (-A_I) \cdot \frac{R_B}{R_B + Z_i}$

$A_{IS} = \frac{-1 \times 10^3}{(1 \times 10^3) + (1.2 \times 10^3)} \times 49.32 \times \frac{1.923 \times 10^3}{(1.923 \times 10^3) + (1.093 \times 10^3)}$

$\therefore A_{IS} = -14.29$

⇒ In the common collector amplifier shown in below, the transistor parameters are $h_{ic} = 1.2k\Omega$, $h_{fc} = -101$, $h_{rc} = 1$, $h_{oc} = 25\mu A/V$, Calculate A_I, Z_i, A_V, Y_o, A_{IS}, A_{VS} for the circuit using exact analysis



Sol⇒ Given $h_{ic} = 1.2k\Omega$, $h_{fc} = -101$, $h_{rc} = 1$, $h_{oc} = 25\times10^{-6}$ ℧

$R_1 = 10k\Omega$, $R_2 = 10k\Omega$, $R_E = 5k\Omega$, $R_L = 20k\Omega$

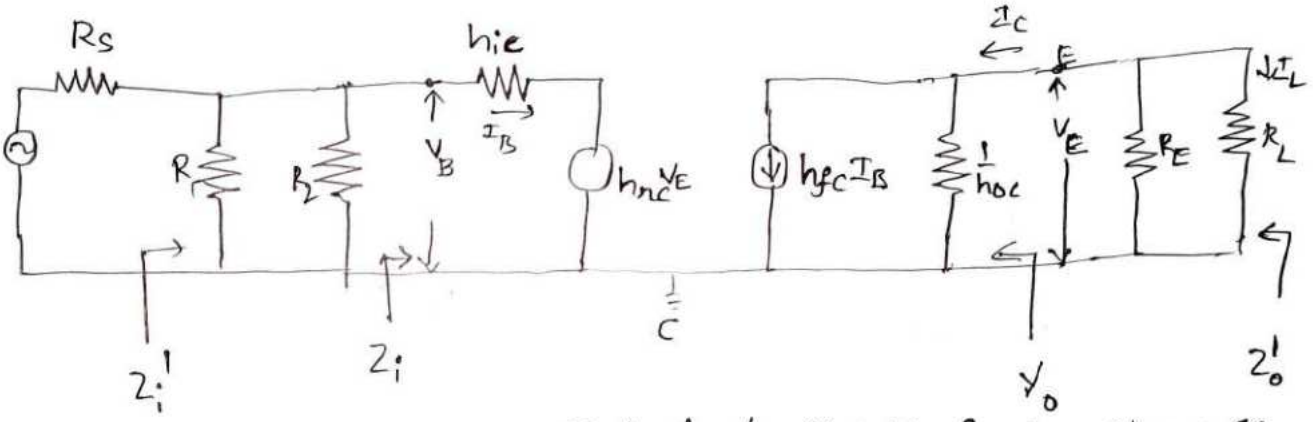


fig: H-parameter equivalent circuit for the given CC amplifier

↳ Current Gain $A_I = \dfrac{-h_{fc}}{1 + h_{oc} R_L'}$ where $R_L' = R_E \| R_L$

$R_L' = 5k\Omega \| 20k\Omega$

$R_L' = 4k\Omega$

$= \dfrac{-(-101)}{1 + (25\times10^{-6} \times 4\times10^{3})}$

$= 91.81$

↳ Input Impedance $Z_i = h_{ic} + h_{rc} A_I R_L'$

$= 1200 + (1)(91.81)(4000)$

$Z_i = 368.472\ k\Omega$

overall input impedance $Z_i' = Z_i \| R_1 \| R_2$

$= 368.472k\Omega \| 10k\Omega \| 10k\Omega$

$= 368.472\text{k}\Omega \parallel 5\text{k}\Omega$

$\therefore Z_i' = 4.933\ \text{k}\Omega$

↳ voltage Gain $A_V = \dfrac{A_I R_L'}{Z_i} = \dfrac{(91.81)(4000)}{368.472 \times 10^3}$

$\therefore A_V = 0.9967$

↳ output admittance $Y_o = h_{oc} - \dfrac{h_{rc} h_{fc}}{R_S' + h_{ic}}$

where $R_S' = R_S \parallel R_1 \parallel R_2 = 1\text{k}\Omega \parallel 10\text{k}\Omega \parallel 10\text{k}\Omega$

$\Rightarrow R_S' = 833.33\Omega$

$\therefore Y_o = 25 \times 10^{-6} - \dfrac{1.(-101)}{833.33 + 1200}$

$Y_o = 0.0497\ \mho$

output Impedance $Z_o = \dfrac{1}{Y_o} = \dfrac{1}{0.0497} = 20.1219\Omega$

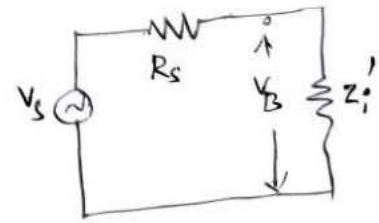
overall output Impedance $Z_o' = Z_o \parallel R_E \parallel R_L = Z_o \parallel R_L'$

$\Rightarrow Z_o' = 20.1219 \parallel 4000$

$\Rightarrow Z_o' = 20.02\Omega$

↳ Voltage Gain with source $(A_{VS}) = \dfrac{V_E}{V_S} = \dfrac{V_E}{V_B} \cdot \dfrac{V_B}{V_S} = A_V \cdot \dfrac{V_B}{V_S}$

$\Rightarrow A_{VS} = A_V \cdot \dfrac{\left(\dfrac{V_S \cdot Z_i'}{R_S + Z_i'}\right)}{V_S}$



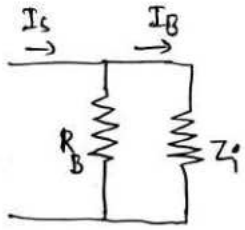
$\Rightarrow A_{VS} = \dfrac{A_V Z_i'}{R_S + Z_i'}$

$= \dfrac{0.9967 \times 4.933 \times 10^3}{1000 + 4933}$

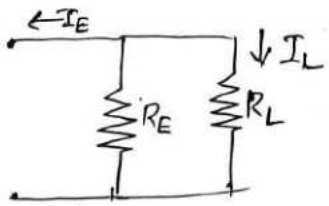
$\therefore A_{VS} = 0.8287$

∴ voltage Gain with source (A_{VS}) = 0.8287

→ Current Gain with source $(A_{IS}) = \frac{I_L}{I_S}$



fig(a)



fig(b)

$$A_{IS} = \frac{I_L}{I_E} \cdot \frac{I_E}{I_B} \cdot \frac{I_B}{I_S}$$

$$A_{IS} = \frac{I_L}{I_E} \cdot (-A_I) \cdot \frac{I_B}{I_S} \rightarrow (1) \qquad \left(\because A_I = \frac{-I_E}{I_B}\right)$$

From fig(a) $I_B = \frac{I_S R_B}{R_B + Z_i}$

$$\Rightarrow \frac{I_B}{I_S} = \frac{R_B}{R_B + Z_i} = \frac{5\times10^3}{5\times10^3 + (368.44\times10^3)} \qquad \left(\begin{array}{l} R_B = R_1 \| R_2 \\ = 10k\Omega \| 10k\Omega \\ = 5k\Omega \end{array}\right)$$

$$\Rightarrow \frac{I_B}{I_S} = 0.0134 \rightarrow (2)$$

From fig(b) $I_L = \frac{-I_E \cdot R_E}{R_E + R_L}$

$$\Rightarrow \frac{I_L}{I_E} = \frac{-R_E}{R_E + R_L} = \frac{-5\times10^3}{5\times10^3 + 20\times10^3}$$

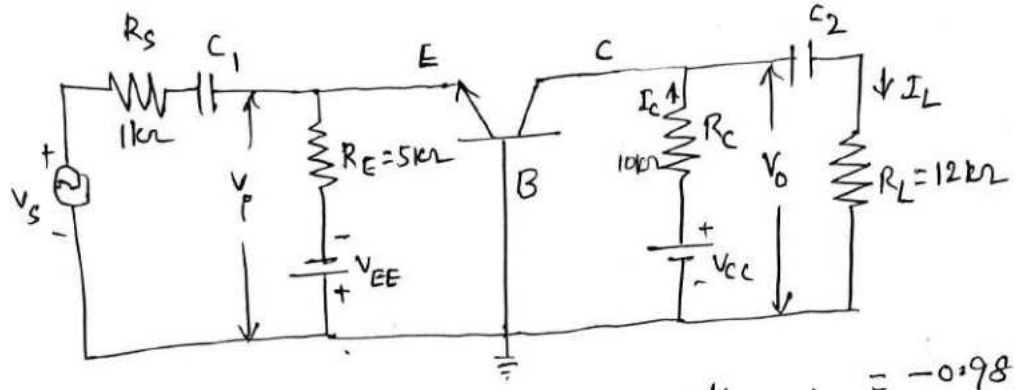
$$\Rightarrow \frac{I_L}{I_E} = -0.2 \rightarrow (3)$$

substitute eq (3), (2) in eq (1) along with $A_I = 91.81$

we get $A_{IS} = (-0.2)(-91.81)\cdot(0.0134)$

$\therefore A_{IS} = 0.2461$

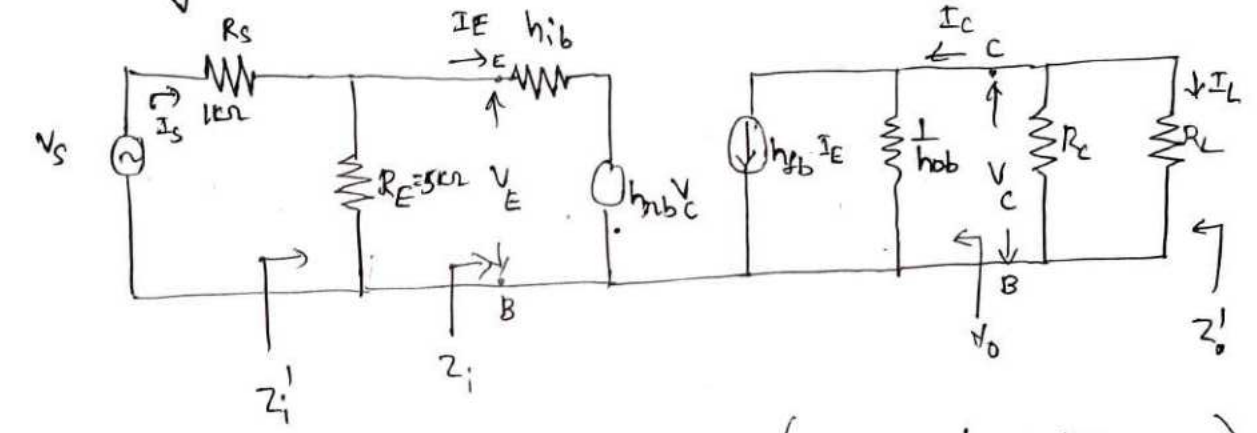
3) From the common base amplifier the transistor parameters are $h_{ib} = 22\Omega$, $h_{fb} = -0.98$, $h_{ob} = 0.49\,\mu A/V$, $h_{rb} = 2.9\times10^{-4}$. Calculate the values of Current gain, input impedance, voltage gain output admittance, voltage gain with source and Current gain with source using exact analysis



Sol) Given $h_{ib} = 22\Omega$, $h_{rb} = 2.9\times10^{-4}$, $h_{fb} = -0.98$, $h_{ob} = 0.49\,\mu A/V$

$R_S = 1k\Omega$, $R_E = 5k\Omega$, $R_C = 10k\Omega$, $R_L = 12k\Omega$.

The H-parameter equivalent circuit for the given circuit is given in below figure.



↳ Current Gain $(A_I) = \dfrac{-h_{fb}}{1+h_{ob}R_L'}$ (where $R_L' = R_C \| R_L$)

$= 10k\Omega \| 12k\Omega$

$R_L' = 5.4545k\Omega$

$$= \frac{-(-0.98)}{1+(0.49\times10^{-6}\times5.4545\times10^{3})}$$

$$= +0.9774$$

$\therefore A_I = 0.9774$

↳ Input Impedance $(Z_i) = h_{ib} + h_{rb}A_I R_L'$

$$= 22 + (2.9\times10^{-4}\times0.9774\times5.4545\times10^{3})$$

$Z_i = 23.5448\Omega$

Overall input Impedance $Z_i' = R_E \| Z_i$

$= 5k\Omega \| 23.5448$

$\therefore Z_i' = 23.4344\Omega$

↳ voltage Gain $(A_V) = \dfrac{A_I R_L'}{Z_i}$

$$= \frac{0.9774 \times (5.4545 \times 10^{3})}{23.5448}$$

$$\therefore A_V = 226.4291$$

↳ output admittance $Y_o = h_{ob} - \dfrac{h_{rb} h_{fb}}{R_S' + h_{ib}}$

where $R_S' = R_S \| R_E = 1K\Omega \| 5K\Omega = 833.33\Omega$

$$\therefore Y_o = 0.49 \times 10^{-6} - \frac{2.9 \times 10^{-4} \times (-0.98)}{833.3 + 22}$$

$$= 0.49 \times 10^{-6} + 0.33 \times 10^{-6}$$

$$Y_o = 0.82 \times 10^{-6} \, \mho$$

The output Impedance $Z_o = \dfrac{1}{Y_o} = \dfrac{1}{0.82 \times 10^{-6}} = 1.21 M\Omega$

over all output impedance $(Z_o') = Z_o \| R_C \| R_L = 1.21 \times 10^{6} \| R_L'$ $(\because R_C \| R_L = R_L')$

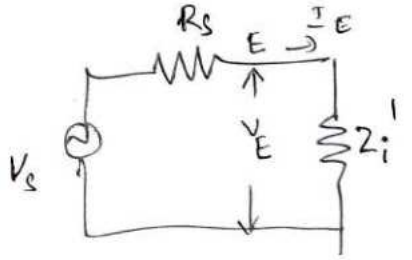
$$= 1.21 \times 10^{6} \| 5.4545 \times 10^{3}$$

$$= 5.43 K\Omega$$

↳ Voltage Gain with source (A_{VS})

$$A_{VS} = \frac{V_C}{V_S} = \frac{V_C}{V_E} \cdot \frac{V_E}{V_S}$$

$$\Rightarrow A_{VS} = A_V \cdot \frac{V_E}{V_S}$$



from this figure $V_E = \dfrac{V_S \cdot Z_i'}{R_S + Z_i'}$

$$\Rightarrow \frac{V_E}{V_S} = \frac{Z_i'}{R_S + Z_i'} = \frac{23.4344}{1000 + 23.4344} = 0.0229$$

$$\therefore A_{VS} = A_V \cdot \frac{V_E}{V_S} = 226.4291 \times 0.0229 = 5.1847$$

∴ Voltage Gain with source $(A_{VS}) = 5.1847$

Current Gain with source (A_{IS}) :

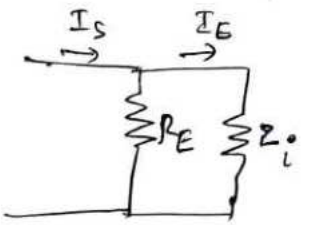


fig (a):

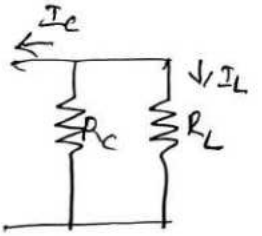


fig (b)

$$A_{IS} = \frac{I_L}{I_S} = \frac{I_L}{I_C} \cdot \frac{I_C}{I_E} \cdot \frac{I_E}{I_S}$$

$$= \frac{I_L}{I_C}\left[\left(\frac{-I_C}{I_E}\right)\right]\frac{I_E}{I_S} \qquad \left(\because \frac{-I_C}{I_E} = A_I\right)$$

$$A_{IS} = -\frac{I_L}{I_C}(A_I)\frac{I_E}{I_S} \longrightarrow (1)$$

from fig (b) $I_L = \frac{-I_C R_C}{R_C + R_L} \Rightarrow \frac{-I_L}{I_C} = \frac{R_C}{R_C + R_L}$

$$\Rightarrow -\frac{I_L}{I_C} = \frac{10k\Omega}{10k\Omega + 12k\Omega} = 0.4545 \longrightarrow (2)$$

from fig (a) $I_E = \frac{I_S \cdot R_E}{R_E + Z_i} \Rightarrow \frac{I_E}{I_S} = \frac{R_E}{R_E + Z_i}$

$$= \frac{5\times10^3}{(5\times10^3) + 23.5248}$$

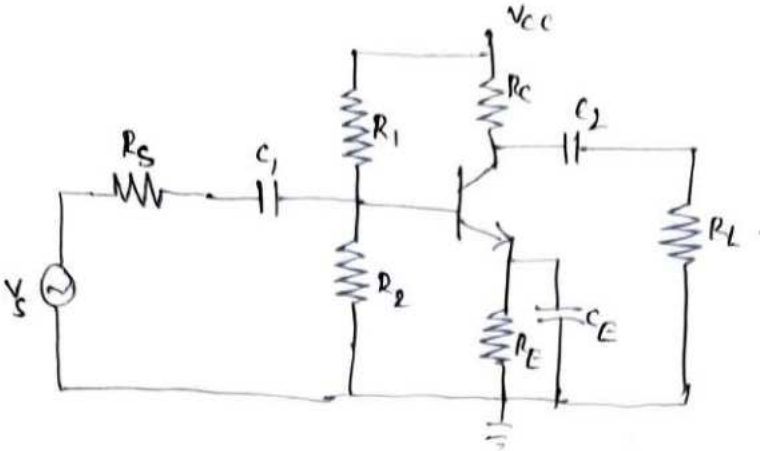
$$\frac{I_E}{I_S} = 0.9953 \longrightarrow (3)$$

Substitute $A_I = 0.9774$, eq (2), eq (3) in eq (1) we get

$$A_{IS} = 0.4545 \times 0.9774 \times 0.9953$$

$$\therefore A_{IS} = 0.4421$$

4) Consider a single stage CE amplifier with $R_S = 1k\Omega$, $R_1 = 50k\Omega$, $R_2 = 2k\Omega$, $R_C = 2k\Omega$, $R_L = 2k\Omega$, $h_{fe} = 50$, $h_{ie} = 1.1k\Omega$, $h_{oe} = 25\times10^{-6}$ A/V $h_{re} = 2.5\times10^{-4}$ as shown in below figure. Find A_I, Z_I, A_V, Y_o and R_o



Sol) Given $R_S = 1k\Omega$, $R_1 = 50k\Omega$, $R_2 = 2k\Omega$, $R_C = 2k\Omega$, $R_E = 2k\Omega$, $h_{ie} = 1.1k\Omega$, $h_{fe} = 50$, $h_{re} = 2.5\times10^{-4}$ $h_{oe} = 25\times10^{-6}$ A/V

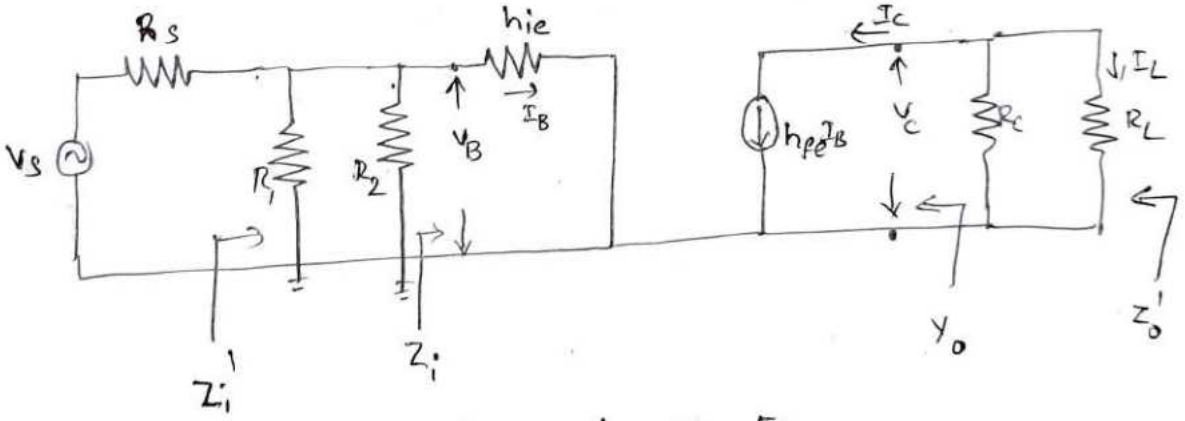
The given circuit has a transistor with $h_{oe} = 25\times10^{-6}$ A/V and $R_L = 2k\Omega$,

$$h_{oe}\cdot R_L' = 25\times10^{-6}\times\left(2\times10^3 \,||\, 2/10^3\right)$$

$$= 25\times10^{-6}\times 1\times10^3$$

$$= 0.025$$

$\therefore h_{oe}R_L' < 0.1$ so we go for approximate analysis



↳ The current gain $(A_I) = -h_{fe} = -50$

↳ Input impedance $Z_i = h_{ie} = 1.1k\Omega$

↳ voltage gain $(A_V) = \dfrac{A_I R_L'}{Z_i} = \dfrac{(-50)(1\times10^3)}{1.1\times10^3}$ $\left(\because R_L' = R_C \,||\, R_L = 2k\Omega \,||\, 2k\Omega = 1k\Omega\right)$

$\Rightarrow A_V = -45.45$

↳ overall input impedance $Z_i' = Z_i \,||\, R_1 \,||\, R_2$

$= 1.1\times10^3 \,||\, 50\times10^3 \,||\, 2\times10^3$

$$\Rightarrow \quad Z_i' = 1.1\times10^3 \,||\, 1.923\times10^3$$

$$Z_i' = 699.7\ \Omega$$

↳ output admittance $(Y_o) = 0$

output impedance $(Z_o) = \frac{1}{Y_o} = \frac{1}{0} = \infty$

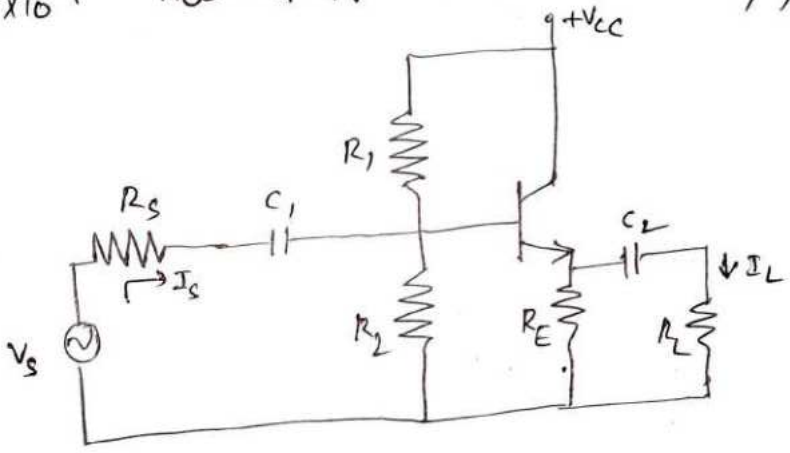
overall output impedance $Z_o' = Z_o \,||\, R_E \,||\, R_L$

$$= \infty \,||\, 2k\Omega \,||\, 2k\Omega$$

$$= \infty \,||\, 1k\Omega$$

$$\therefore Z_o' = 1k\Omega$$

5) Consider a common collector amplifier that has $R_1 = 27k\Omega$, $R_2 = 27k\Omega$, $R_E = 5.6k\Omega$, $R_L = 47k\Omega$, $R_S = 600\Omega$, $h_{ie} = 1k\Omega$, $h_{fe} = 85$ $h_{re} = 2.5\times10^{-4}$ $h_{oe} = 2\mu A/V$ Calculate A_I, R_i, A_V, Y_o



Sol) Given $R_1 = 27k\Omega$, $R_2 = 27k\Omega$, $R_E = 5.6k\Omega$, $R_L = 47k\Omega$, $R_S = 600\Omega$, $h_{ie} = 1k\Omega$, $h_{fe} = 85$, $h_{oe} = 2\mu A/V$, $h_{re} = 2.5\times10^{-4}$

$$h_{oe} R_L' = 2\times10^{-6} \times (R_E \,||\, R_L)$$

$$= 2\times10^{-6} \times (5.6\times10^3 \,||\, 47\times10^3)$$

$$= 2\times10^{-6} \times 5.003\times10^3$$

$$= 0.01$$

$h_{oe} R_L' < 0.1$ so we go for approximate analysis

Current Gain $(A_I) = 1 + h_{fe} = 1 + 85 = 86$

Input Impedance $Z_i = h_{ie} + (1 + h_{fe}) R_L'$

$= 1\times10^3 + (1+85)(5.003\times10^3)$

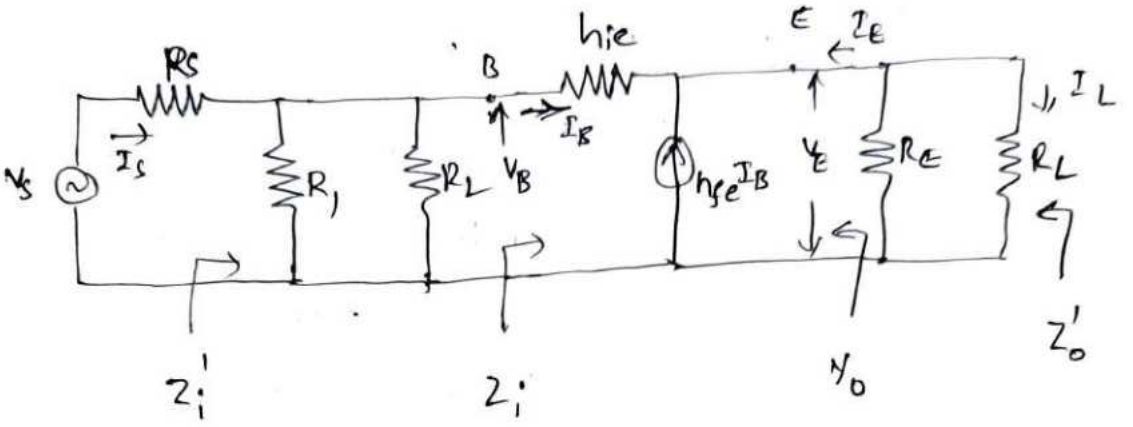
$= 431.258\ k\Omega$

over all input impedance $Z_i' = R_1 \| R_2 \| Z_i$

$= 27\times10^3 \| 27\times10^3 \| 431.258\times10^3$

$= 13.5\times10^3 \| 431.258\times10^3$

$Z_i' = 13.09\ k\Omega$



↳ voltage gain $(A_v) = \dfrac{(1+h_{fe})R_L'}{h_{ie} + (1+h_{fe})R_L'}$

$= \dfrac{(1+85)(5.003\times10^3)}{1000 + (1+85)(5.003\times10^3)}$

$A_v = 0.9977$

↳ output Admittance $Y_o = \dfrac{1+h_{fe}}{R_s' + h_{ie}} = \dfrac{1+85}{(R_s \| R_1 \| R_2) + (1\times10^3)}$ (where $R_s' = R_1 \| R_2 \| R_s$)

$R_s = 600\ \Omega$, $R_1 = 27k\Omega$, $R_2 = 27k\Omega$, $R_1 \| R_L = 13.5k\Omega$

$\therefore R_s' = 13.5\ k\Omega \| 600 = 574.468\ \Omega$

$\therefore Y_o = \dfrac{1+85}{574.468 + 1000} = 0.0546$

output Impedance $z_o = \dfrac{1}{Y_o} = \dfrac{1}{0.0546} = 18.30\ \Omega$

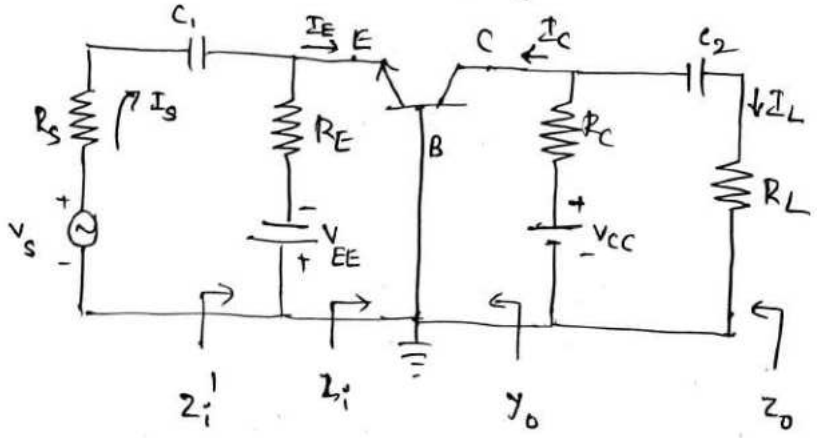
overall output Impedance $Z_o' = Z_o \| R_E \| R_L$

$= 18.3 \| 5.6\times10^3 \| 47\times10^3$

$\therefore Z_o' = 18.233\ \Omega$

c) A common base amplifier has the components $R_s = 600\,\Omega$, $R_C = 5.6\,k\Omega$, $R_E = 5.6\,k\Omega$, $R_L = 39\,k\Omega$, $h_{ie} = 1k\Omega$ $h_{fe} = 85$, $h_{oe} = 2\mu A/V$

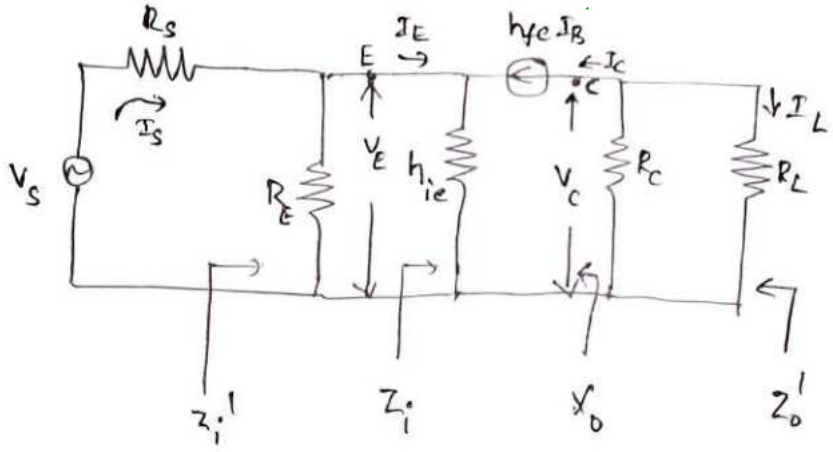
Calculate A_I, Z_i, A_V, Y_o



sol) since $h_{oe} R_L' = 2\times10^{-6} \times (R_C \| R_E) = 2\times10^{-6} \times (5.6k\Omega \| 39.k\Omega)$

$= 9.79\times10^{-3}$

$\Rightarrow h_{oe} R_L' = 0.00979 < 0.1$ we go for approximate analysis



↳ Current Gain $A_I = \frac{h_{fe}}{1+h_{fe}} = \frac{85}{1+85} = 0.9884$

↳ Input impedance $(Z_i) = \frac{h_{ie}}{1+h_{fe}} = \frac{1\times10^3}{1+85} = 11.6279\,\Omega$

overall input impedance $(Z_i') = Z_i \| R_E = 11.6279 \| 5.6\times10^3$

$\therefore Z_i' = 11.60\,\Omega$

↳ voltage Gain $(A_V) = \frac{h_{fe} R_L'}{h_{ie}} = \frac{85 \times (39\times10^3 \| 5.6\times10^3)}{1\times10^3} = 416.23\,\Omega$

$(\because R_L' = R_L \| R_C)$

↳ output admittance $Y_0 = 0$

output impedance $Z_0 = \frac{1}{Y_0} = \frac{1}{0} = \infty$

overall output impedance $Z_0' = Z_0 \| R_L' = Z_0 \| R_c \| R_L$

$\Rightarrow Z_0' = \infty \| 5.6k\Omega \| 39k\Omega = 4.896k\Omega$

Miller's Theorem:

In general, the miller's theorem is used for converting any circuit having the configuration shown in figure(a) to another configuration shown in figure(b).

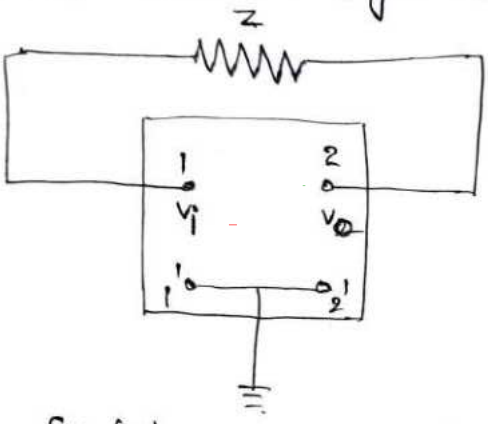
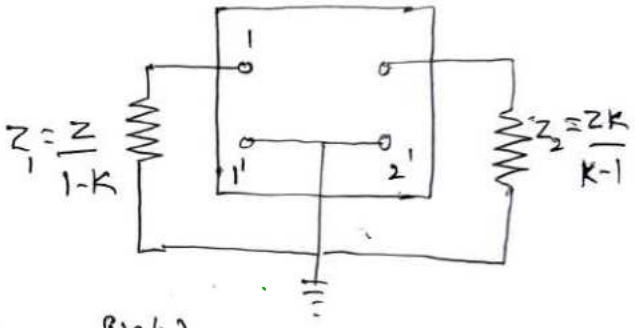


fig (a)



fig(b)

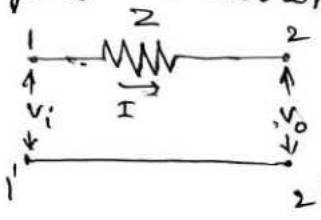
The above figures shows that, if the impedance 'Z' is connected between two nodes, node1 and node 2 it can be replaced by two seperate impedances Z_1 and Z_2 where Z_1 is connected between node 1 and ground and Z_2 is connected between Node 2 and Ground.

V_i and V_o are the voltages at node1 and node 2 with respect to Ground respectively. The values of Z_1 and Z_2 are derived from the ratio of V_o and V_i. Thus it is important to know the values of V_i and V_o to calculate Z_1 and Z_2.

proof:

Miller's theorem states that the effect of impedance 'Z' on the input circuit is a ratio of input voltage to the current I which flows from input to output

$\therefore Z_1 = \frac{V_i}{I} \Rightarrow Z_1 = \frac{V_i}{\left(\frac{V_i - V_o}{Z}\right)}$

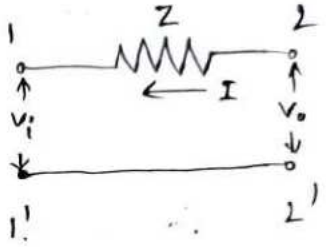


$$\Rightarrow \quad Z_1 = \frac{Z V_i}{V_i - V_o}$$

$$= \frac{Z V_i}{V_i \left(1 - \frac{V_o}{V_i}\right)}$$

$$\Rightarrow \boxed{Z_1 = \frac{Z}{1-K}} \qquad \text{where } K = \frac{V_o}{V_i}$$

Miller's theorem states that the effect of impedance on the output circuit is the ratio of the output voltage to the current flows from the output to the input.



$$Z_2 = \frac{V_o}{I}$$

$$\Rightarrow Z_2 = \frac{V_o}{\left(\frac{V_o - V_i}{Z}\right)}$$

$$\Rightarrow Z_2 = \frac{Z V_o}{V_o - V_i} = \frac{Z V_o}{V_o\left(\frac{V_o}{V_o} - \frac{V_i}{V_o}\right)} = \frac{Z}{1 - \frac{1}{(V_o/V_i)}}$$

$$\Rightarrow \quad Z_2 = \frac{Z}{1 - \frac{1}{K}} = \frac{ZK}{K-1}$$

$$\therefore \quad \boxed{Z_2 = \frac{ZK}{K-1}}$$

NOTE:

In the place of Z if we have R, (or) $j\omega L$ (or) $\frac{1}{j\omega C}$ then the following changes will occur

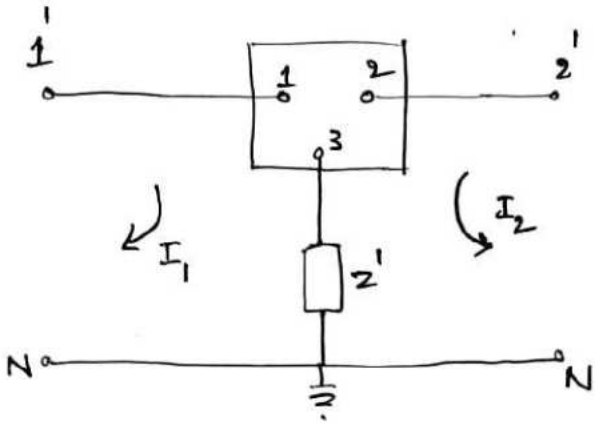
i) If $Z = R$, then $Z_1 = R_1 = \frac{R}{1-K}$ and $Z_2 = R_2 = \frac{RK}{K-1}$

ii) If $Z = j\omega L$ then $Z_1 = L_1 = \frac{L}{1-K}$ and $Z_2 = L_2 = \frac{LK}{K-1}$

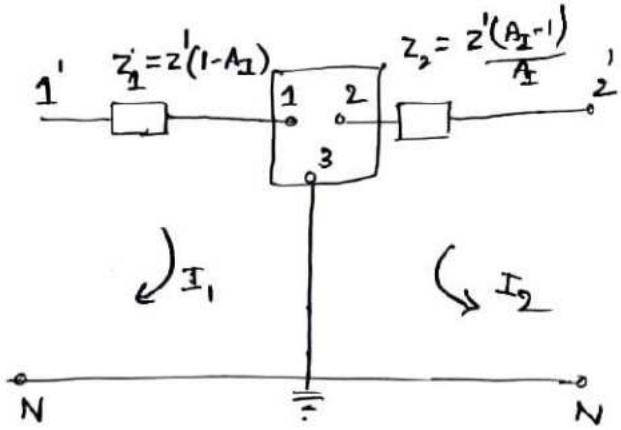
iii) If $Z = \frac{1}{j\omega C}$ then $Z_1 = C_1 = C(1-K)$ & $Z_2 = C_2 = \frac{C(K-1)}{K}$

Dual of Miller's Theorem:

Consider a network shown in figure(a) in which Z' is the impedance between node3 and Ground(N). According to the dual of Miller's theorem Z' can be split into Z_1 and Z_2 such that Z_1 is placed in mesh1 and Z_2 is added to mesh2 as shown in fig(b)



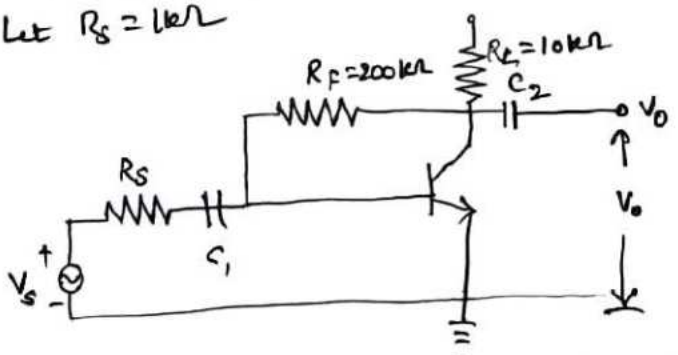
fig(a)



fig(b)

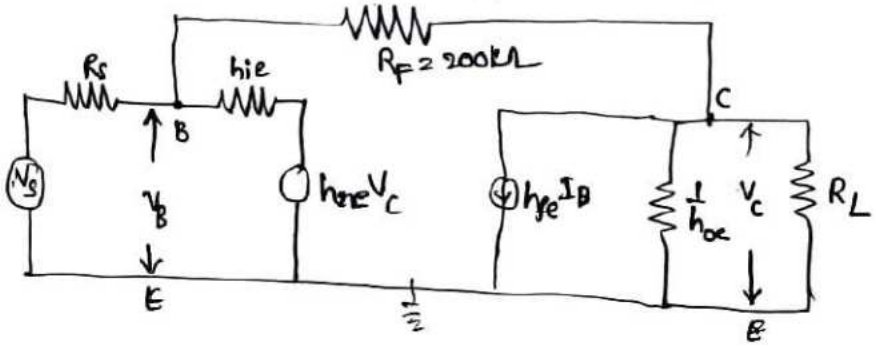
where $A_I = \frac{-I_2}{I_1}$

problem: A Common Emitter Amplifier with Collector to base bias has the transistor h-parameters $h_{ie} = 1.1\,k\Omega$, $h_{fe} = 50$, $h_{oe} = 25\,\mu A/V$, $h_{re} = 2.5\times10^{-4}$ Calculate Z_i, Z_i', A_V, A_I and output impedance for the figure shown below. Let $R_S = 1k\Omega$

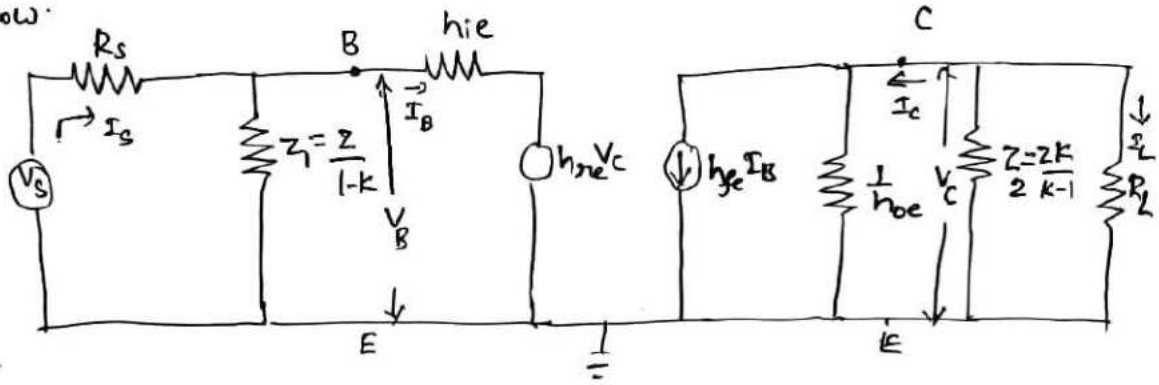


Sol) Given $h_{ie} = 1.1k\Omega$, $h_{fe} = 50$, $h_{oe} = 25\mu A/V$, $h_{re} = 2.5\times10^{-4}$

The h-parameter equivalent model for the given circuit is given below



Using miller's theorem the above circuit can be simplified as shown in below.



From the figure $R_L' = R_L \| Z_2$ where $Z_2 = \frac{Zk}{k-1}$ and $k = \frac{V_c}{V_B}$

The value of Z_2 is not known until k is not known. (i.e $k = A_V$) but k is not known until A_V is not known. Hence we make an assumption such that $Z_2 = \frac{Zk}{k-1} \simeq Z$ i.e $Z_2 = Z = 200k\Omega$

Now $R_L' = R_L \| Z_2 = 10\times10^3 \| 200\times10^3 = 9.523\,k\Omega$

$h_{oe}R_L' = 25\times10^{-6} \times 9.523\times10^3 = 0.238 > 0.1$

Since $h_{oe}R_L' > 0.1$ we go for exact analysis

i) Current Gain $A_I = \frac{-h_{fe}}{1+h_{oe}R_L'} = \frac{-50}{1+(25\times10^{-6}\times9.523\times10^3)} = -40.384$

ii) Input impedance $Z_i = h_{ie} + h_{re}A_I R_L'$

$= 1100 + 2.5\times10^{-4} \times (-40.384) \times 9.523\times10^3$

$Z_i = 1003.855\,\Omega$

over all input impedance $Z_i' = Z_1 \| Z_i$ but to find Z_1 we require k i.e voltage gain A_V.

iii) Voltage Gain $(A_V) = \frac{A_I R_L'}{Z_i} = \frac{-40.384 \times 9.523\times10^3}{1003.855} = -383.1$

$\therefore \quad k = A_V = -383.1$

Now $Z_1 = \frac{Z}{1-k} = \frac{200\times10^3}{1-(-383.1)} = 520.69\,\Omega$

$\therefore$ overall input impedance $Z_i' = Z_1 \| Z_1 = 1003.855 \| 520.69$

$\Rightarrow Z_i' = 342.85\,\Omega$

output admittance $Y_0 = h_{oe} - \dfrac{h_{re}h_{fe}}{h_{ie} + R_s'}$

where $R_s' = R_s \| Z_1 = 1\times10^3 \| 520.69 = 342.4038\,\Omega$

$\therefore Y_0 = 25\times10^{-6} - \dfrac{2.5\times10^{-4}\times50}{1100 + 342.4038}$

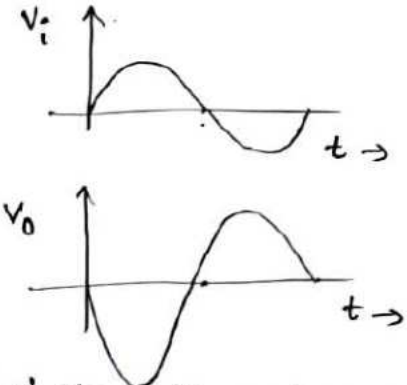
$= 25\times10^{-6} - 8.8\times10^{-6}$

$= 16.2\times10^{-6}\,\mho$

output impedance $(Z_0) = 1/Y_0 = \dfrac{1}{16.2\times10^{-6}} = 61.728\,k\Omega$

Characteristics of CE amplifier:

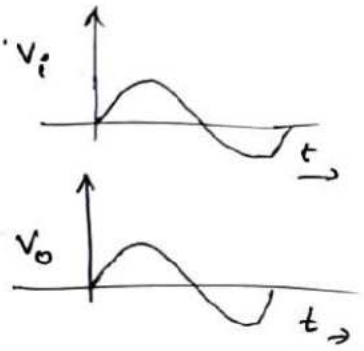
i) Larger current gain (A_I)
ii) Large voltage Gain (A_V)
iii) Large power Gain ($A_p = A_I \cdot A_V$)
iv) Voltage Phase shift of 180° between input and output.
v) moderate input impedance
vi) Moderate output impedance



i/p & o/p voltages of CE amplifier

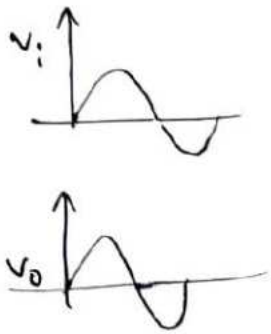
Characteristics of CC amplifier:

i) Large current Gain
ii) Voltage gain is approximately unity
iii) Power Gain is approximately equal to current Gain
iv) No Phase shift between i/p voltage and o/p voltage.
v) Large input impedance
vi) Small output impedance.



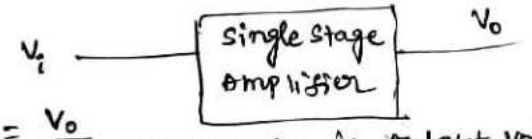
Characteristics of CB amplifier:

i) Current Gain is less than unity
ii) Voltage gain is high
iii) power Gain is approximately equal to voltage Gain
iv) No Phase Shift between input and o/p voltage
v) Small input impedance
vi) Large output impedance.



Single stage amplifier:

An amplifier in which the amplification is done only in a single stage is called as single stage amplifier.



Gain (A_V) = $\frac{V_o}{V_o}$ where V_o is output voltage and V_i is input voltage

Multistage Amplifier:

For a pratical application if the voltage gain (or) Power gain obtained from a single stage small signal amplifier is not sufficient, one can use more than one stage of amplifiers to achieve the necessary voltage gain and power gain. Such an amplifier is called a multistage amplifier.

In a multistage amplifier, the output of one stage is fed as the input to the next stage as shown in below figure, such a connection is called as cascading.

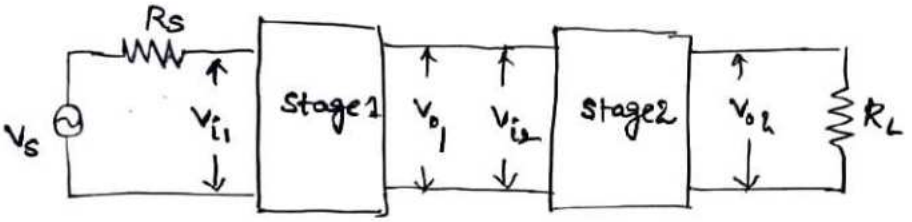


fig: Block diagram of a two stage cascaded amplifier.

In amplifiers, cascading is also done to achieve correct input and output impedances for specific applications. Depending upon the type of the amplifier used in each individual stage, multistage amplifier can be classified into several types.

A multistage amplifier having two or more single stage CE amplifiers is called as Cascade Amplifiers.

A multistage amplifier with a CE amplifier as a first stage and CB amplifier as the 2nd stage is called as a cascode amplifier. Such cascade and cascode amplifiers are also possible with Field Effect transistor amplifiers.

Coupling schemes used in amplifiers:

When amplifiers are cascaded, it is necessary to use a coupling network between the output of one stage and the input of the following stage. This type of coupling is called interstage coupling.

Basically the coupling network serves the following purposes.

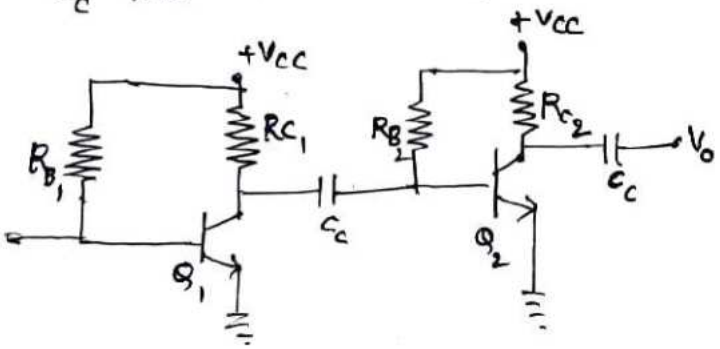
1) It transfers the AC output of one stage to the input of the next stage.

2) It isolates the DC components from the output of one stage and does not let them to reach the next stage.

There are three coupling schemes that are commonly used in multistage amplifiers. They are

1) Rc coupling 2) Transformer coupling 3) Direct coupling.

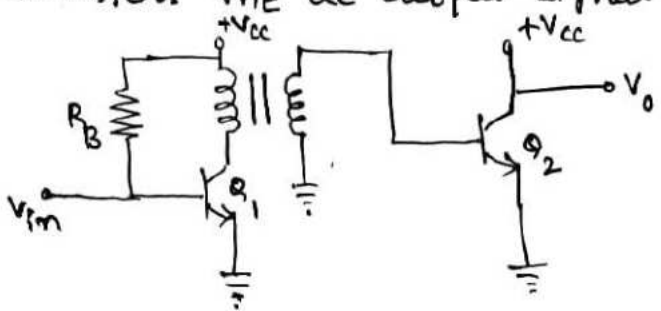
1) Rc coupling : It is the most commonly used coupling technique as it is less expensive. In this method, the signal developed across the collector resistor R_c of each stage is coupled through a capacitor C_c into the base of the next stage as shown in figure below.



The amplifier that uses Rc coupling is called as RC coupled amplifier. The coupling capacitor C_c isolates the DC components of one stage from it's following stage.

The RC network gives a wide band frequency response without peak at any frequency. However it's frequency response drops off at very low frequencies due to coupling capacitors and also at high frequencies due to internal capacitances of the transistors.

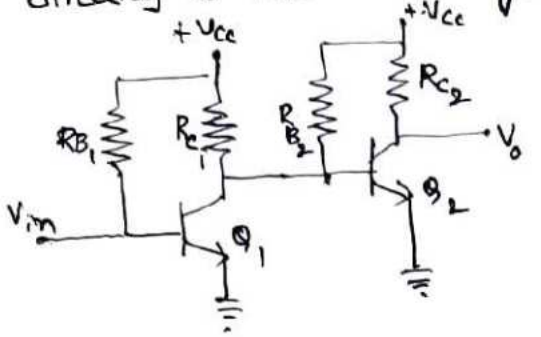
2) Transformer Coupling : In this method, the primary winding of the transformer acts as the collector load and the secondary winding transfers the ac output signal directly to the base of the next stage, as shown in below figure.



Such coupling is very useful in providing impedance matching. However transformer with broad

frequency response are expensive and hence this type of coupling is restricted to power amplifiers where impedance - matching is the critical requirement for maximum power transfer and efficiency. The amplifiers using this transformer coupling are called as transformer coupled amplifiers.

3) Direct coupling: In this method, the ac output signal is fed directly to the next stage as shown in figure below. The amplifier that uses direct coupling is called as direct coupled amplifier. This coupling is preferred when amplification of low frequency signal is required.



Frequency response of an RC coupled amplifier:

The frequency response of any amplifier is a plot between the magnitude of gain (usually voltage gain) and frequency. To plot the frequency response it is better to use the logarithmic scale on x-axis to permit various frequencies in a frequency range.

In general the entire frequency range is divided into three ranges. i) Mid band frequency range ii) Low frequency - range iii) High frequency range.

Mid band frequency range:

In this frequency range the voltage gain is practically constant, that is not affected by the changes of capacitances in the circuit. The reactance $\frac{1}{\omega C_c}$ of the coupling capacitor is in series between the output of a stage and the input of it's next stage, which is very small in this range, so the capacitance C_c is treated as short circuit in this range. The reactances of the internal capacitances of the transistors are very large in this -

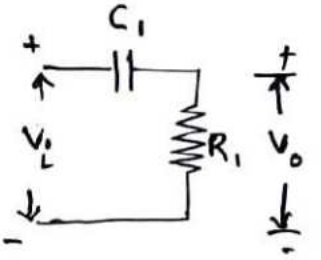
region of frequencies as they have a very small capacitances. These internal capacitances come in parallel with the associated resistances in the circuit, so they are not considered in this mid band frequency range. Thus, in the mid band frequency range all the capacitive reactances are neglected as compared to the associated circuit resistance components.

The voltage gain in the mid band frequency range is denoted by A_{Vmid} and is equal to 1 in this range.

i.e $A_{Vmid} = 1 = 0$ (in dB)

Low frequency range:

In this frequency range, the circuit behaves like a simple high pass RC circuit with a time constant $\tau_1 = R_1C_1$ as shown in figure below.



Therefor voltage gain in low frequency range

$$A_{VL} = \frac{V_o}{V_i} = \frac{R_1}{R_1 + \frac{1}{j\omega C_1}} = \frac{1}{1 - \frac{j}{\omega R_1 C_1}}$$

$$\Rightarrow A_{VL} = \frac{1}{1 - \frac{j}{2\pi R_1 C_1 \cdot f}} \quad (\text{where } \omega = 2\pi f)$$

Let $\frac{1}{2\pi R_1 C_1} = f_L$ then $A_{VL} = \frac{1}{1 - \frac{j f_L}{f}}$

The magnitude of the voltage gain at low frequency range is

$$|A_{VL}| = \frac{1}{\sqrt{1 + \left(\frac{f_L}{f}\right)^2}} \quad \left(\text{where } f_L = \frac{1}{2\pi R_1 C_1}\right)$$

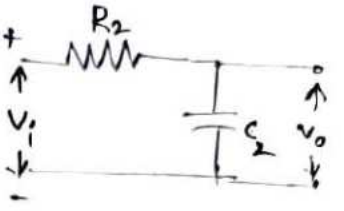
and Phase shift $\theta_1 = -\tan^{-1}\left(\frac{f_L}{f}\right)$

At $f = f_L$ $|A_{VL}| = \frac{1}{\sqrt{2}} = 0.707 = 0.707 A_{Vmid}$ $\left(\because A_{Vmid} = 1\right)$

Therefore the frequency at which the gain is 0.707 times that of

the gain of midband frequency range of the amplifier is called as lower 3dB cut off frequency denoted by f_L

<u>High frequency range:</u> Above the midband frequency ie in the high frequency range the transistor behaves like the simple lowpass RC circuit with time constant $\tau_2 = R_2 C_2$ as shown in below figure.



Therefore the voltage gain at high frequency range is A_{VH} given by

$$A_{VH} = \frac{V_o}{V_i} = \frac{\frac{1}{j\omega C_2}}{R_2 + \frac{1}{j\omega C_2}} = \frac{1}{R_2(j\omega C_2)+1} = \frac{1}{1+jR_2C_2\omega}$$

$$A_{VH} = \frac{1}{1+j2\pi R_2 C_2 f} \quad (\text{where } \omega = 2\pi f)$$

$$A_{VH} = \frac{1}{1+j\left(\frac{f}{f_H}\right)} \quad \left(\text{where } f_H = \frac{1}{2\pi R_2 C_2}\right)$$

The magnitude of voltage gain at high frequency range is

$$|A_{VH}| = \frac{1}{\sqrt{1+\left(\frac{f}{f_H}\right)^2}} \quad \text{and phase shift } \theta_2 = -\tan^{-1}\left(\frac{f}{f_H}\right)$$

At a frequency $f = f_H$, $|A_{VH}| = \frac{1}{\sqrt{2}} = 0.707 = 0.707\, A_{vmid}$

Therefore the frequency in high frequency range at which the gain is 0.707 times the gain of midband frequency range of the amplifier is called as upper 3dB cut off (or) higher 3dB cutoff frequency denoted by f_H.

The frequency range between f_L and f_H is called as the bandwidth of the amplifier. i.e $\boxed{\text{Bandwidth} = f_H - f_L}$

The frequency response of the RC coupled amplifier is as shown in below.

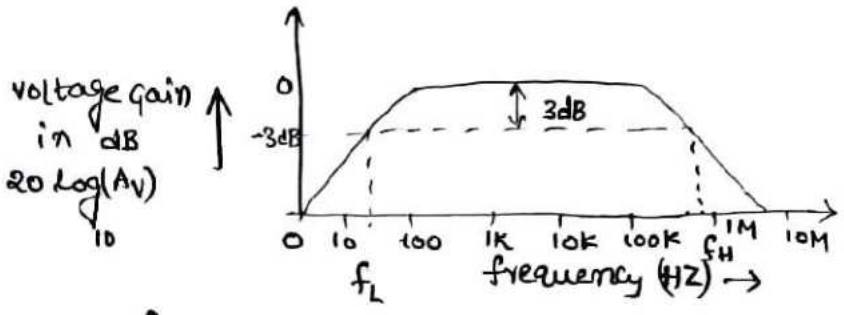


fig: Frequency response of RC coupled amplifier

Gain in decibels (dB): The unit of the logarithmic scale is called decibel abbrevated as dB.

If input power of an amplifier is P_i and output power P_o then the gain (power gain) in dB is $\boxed{A_p = 10 \log_{10}\left(\frac{P_o}{P_i}\right)}$

where $P_i = \frac{V_i^2}{R_i}$, $P_o = \frac{V_o^2}{R_o}$, R_i, R_o are input and output resistances respectively. Therefore $A_p = 10\log_{10}\left(\frac{V_o^2/R_i}{V_i^2/R_o}\right)$

If $R_i = R_o$ then $A_p = 10\log\left(\frac{V_o^2}{V_i^2}\right)$

$\therefore$ Voltage Gain $\boxed{A_v = 20 \log_{10}\left(\frac{V_o}{V_i}\right)}$ dB.

Gain of multistage amplifier

Let the voltage gain of a multistage amplifier is A_V and the voltage gain of the individual stages as $A_{V_1}, A_{V_2}, A_{V_3} \cdots A_{V_n}$

Then $\boxed{A_V = A_{V_1} \cdot A_{V_2} \cdot A_{V_3} \cdots A_{V_n}}$

If the voltage gain (A_V) is required in dB's then

$$20 \log_{10}(A_V) = 20 \log_{10}(A_{V_1} \cdot A_{V_2} \cdot A_{V_3} \cdots A_{V_n})$$

$$A_V(dB) = 20 \log_{10}(A_{V_1}) + 20 \log_{10}(A_{V_2}) + \cdots + 20 \log_{10}(A_{V_n})$$

$\therefore \boxed{A_{V\,dB} = A_{V_1\,dB} + A_{V_2\,dB} + \cdots + A_{V_n\,dB}}$

Advantages of representing gain in dB:

Logarithmic scale is preferred over linear scale to represent voltage gain and power gain because of the following reasons

- In multistage amplifiers the overall gain in dB is calculated by adding the individual gains in dB.
- It allows us to denote both very small as well as very large quantities of gain by considerably small values in dB.

For example voltage gain 0.0000001 can be represented as -140dB and 1,00,000 is represented as 100 dB.

- Many times the output of the amplifier is fed to loud speakers to produce sound which is received by the human ear. It is important to note that the ear responds to the sound intensities on logarithmic scale rather than linear scale. Thus the use of decibel unit is more appropriate for representing gain.

Choice of transistor configuration in multistage amplifiers:

From design point of view we divide the multistage amplifier into three parts : Input stage, middle stages and output stage.

Input stage is designed such that it's input impedance matches with the source impedance and the output stage is designed such that it's output impedance matches with the load impedance. The middle stages are designed to provide the desired gain.

The transistor works as an amplifier in three configurations Common Emitter, Common base and Common Collector.

Assume that the input signal is available with a very low source impedance for a multistage amplifier and with desired gain and the amplifier has to drive the low impedance i.e it has low impedance of load.

We can easily select the common base amplifier as the

input stage. Because the input impedance of common base is very low that matches with the very low impedance of source.

we know that the common Emitter amplifier provides voltage gain as well as current gain hence CE amplifier is the best choice for the middle stages.

The output stage should be selected such that the output impedance should match with the load impedance. In our case output impedance should be low, so we can select the common-collector amplifier as the output stage.

General Analysis of Cascade Amplifier: (or) multistage amplifier:

The most popular cascade amplifier is formed by cascading several CE amplifier stages. Before considering the analysis of any specific type of multistage amplifiers, a general 'n' stage CE amplifier analysis is done here.

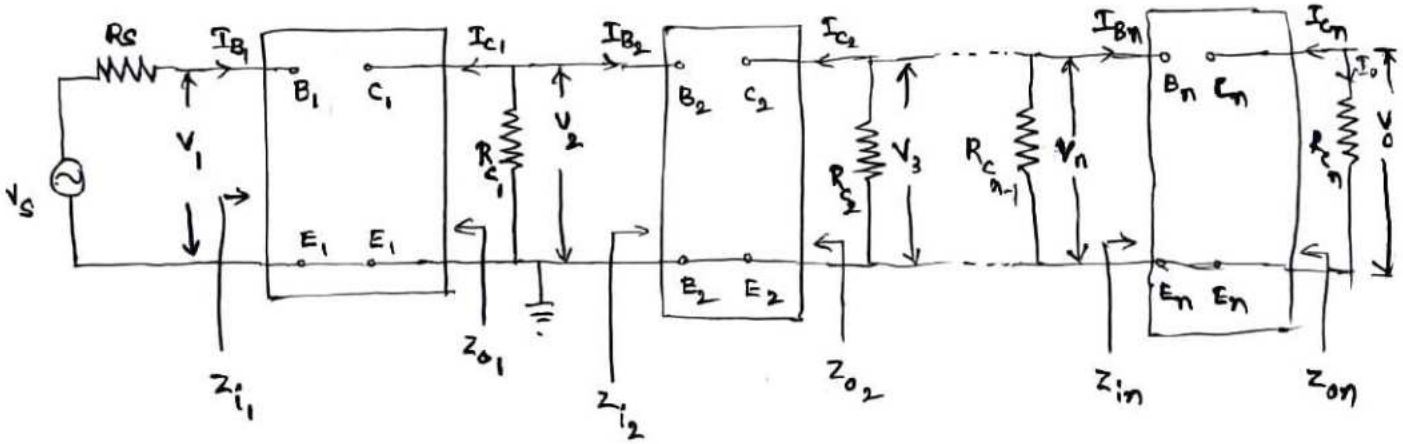


fig: n-stage cascade (or) n-stage CE amplifier

Here the biasing and coupling elements are omitted for simplicity. For the analysis we require the expressions for voltage gain, current gain, input impedance and output impedance for the n-stage CE amplifier.

Voltage Gain: In a multistage amplifier, the output of the first stage acts as the input voltage of the second stage and so on. The voltage gain of the complete n-stage amplifier is equal to the product of the voltage gains of the individual stages.

The voltage gain of the first stage

$$\bar{A}_{V_1} = \frac{\bar{V}_2}{\bar{V}_1} = \frac{\text{output voltage of the first stage}}{\text{Input voltage of the first stage}}$$

$$\therefore \bar{A}_{V_1} = A_{V_1} \angle\theta_1$$

where A_{V_1} is the magnitude of the voltage gain and θ_1 is the phase shift in the output voltage with respect to input voltage V_1.

Similarly $$\bar{A}_{V_2} = \frac{\bar{V}_3}{\bar{V}_2} = \frac{\text{output voltage of the second stage}}{\text{Input voltage of the second stage}}$$

$$\therefore \bar{A}_{V_2} = A_{V_2} \angle\theta_2$$

Similar expressions are written for 'n' stages of the cascade amplifier. The over all resultant voltage gain is

$$\bar{A}_V = \frac{\bar{V}_0}{\bar{V}_1} = \frac{\text{output voltage of the } n^{th} \text{ stage}}{\text{Input voltage of the first stage}}$$

$$\therefore \bar{A}_V = A_V \angle\theta$$

But $$\frac{\bar{V}_0}{\bar{V}_1} = \frac{\bar{V}_0}{\bar{V}_n} \cdot \frac{\bar{V}_n}{\bar{V}_{n-1}} \cdot \frac{\bar{V}_{n-1}}{\bar{V}_{n-2}} \cdots \frac{V_3}{V_2} \cdot \frac{V_2}{V_1}$$

$$\Rightarrow \bar{A}_V = \bar{A}_{V_n} \cdot \bar{A}_{V_{n-1}} \cdot \bar{A}_{V_{n-2}} \cdots \bar{A}_{V_2} \cdot \bar{A}_{V_1}$$

$$\Rightarrow \bar{A}_V = \bar{A}_{V_1} \cdot \bar{A}_{V_2} \cdot \cdots \bar{A}_{V_{n-2}} \bar{A}_{V_{n-1}} \cdot \bar{A}_{V_n} \longrightarrow (1)$$

$$\Rightarrow A_V \angle\theta = A_{V_1} \angle\theta_1 \cdot A_{V_2} \angle\theta_2 \cdot A_{V_3} \angle\theta_3 \cdots A_{V_n} \angle\theta_n$$

$$\Rightarrow A_V \angle\theta = A_{V_1} \cdot A_{V_2} A_{V_3} \cdots A_{V_n} \angle\theta_1 + \theta_2 + \theta_3 \cdots + \theta_n$$

$$\longrightarrow (2)$$

Hence $$A_V = A_{V_1} \cdot A_{V_2} \cdots A_{V_n}, \quad \theta = \theta_1 + \theta_2 + \theta_3 + \cdots + \theta_n$$

From this we can conclude that the voltage gain of n-stage amplifier has a magnitude of A_V which is equal to the magnitude product of the voltage gains of individual stages. And the phase shift of the n-stage amplifier is equal to the sum of the phase shifts of the individual stages.

The voltage gain of a particular stage say k^{th} stage is given by $\bar{A}_{VK} = \dfrac{\bar{A}_{IK} R_{LK}}{Z_{iK}}$ → (3)

where R_{LK} is the effective load impedance at the collector of k^{th} stage and Z_{iK} is the input impedance for that stage. The following figure shows the k^{th} stage of n-stage cascaded amplifier.

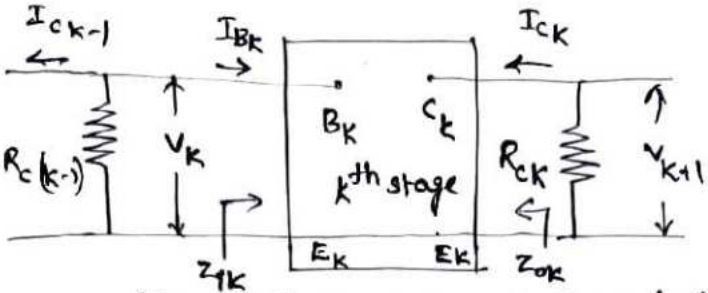


fig: k^{th} stage of a cascaded amplifier.

The terms $\bar{A}_{IK}$, R_{LK} and Z_{iK} are evaluated by starting from the last stage and proceeding towards the first stage.

So the current gain for n^{th} stage $A_{In} = \dfrac{-h_{fe}}{1+h_{oe}R_{Ln}}$

where R_{Ln} is the effective load impedance of n^{th} stage and is equal to R_{cn}.

Having known A_{In}, R_{Ln} we can get input impedance for n^{th} stage $Z_{i(n)}$ i.e $Z_{i(n)} = h_{ie} + h_{re} A_{In} R_{Ln}$

Now Effective load impedance for $n-1^{th}$ stage is $R_{L(n-1)} = R_{C(n-1)} \| Z_{i(n)}$

After getting $R_{L(n-1)}$ find $A_{I(n-1)}$ using $A_{I(n-1)} = \dfrac{-h_{fe}}{1+h_{oe}R_{L(n-1)}}$

After knowing $R_{L(n-1)}$ and $A_{I(n-1)}$ find $Z_{i(n-1)}$ using

$$Z_{i(n-1)} = h_{ie} + h_{re} A_{I(n-1)} R_{L(n-1)}$$

By proceeding in this manner we can find the input impedance of each stage until the first stage along with the effective load impedance and current gain of each stage.

Substituting the current gain, effective load impedance and

input impedance of each stage in eq ③ we get the voltage gain for that stage.

Current Gain:

In order to find the resultant voltage gain, the voltage gains of the individual stages are found out and the product of these gains gives the resultant voltage gain.

Alternatively the resultant voltage gain is calculated by using $\bar{A}_V = \frac{\bar{A}_I R_{in}}{Z_{i1}}$

where $\bar{A}_I$ = Current gain of the Complete n-stage amplifier given by $\bar{A}_I = \frac{\bar{I}_o}{I_{B_1}} = -\frac{\bar{I}_{cn}}{I_{B_1}}$

$$-\frac{\bar{I}_{cn}}{I_{B_1}} = -\frac{\bar{I}_{c_1}}{\bar{I}_{B_1}} \frac{\bar{I}_{c_2}}{\bar{I}_{c_1}} \frac{\bar{I}_{c_3}}{\bar{I}_{c_2}} \cdots \frac{\bar{I}_{cn}}{\bar{I}_{cn-1}}$$

$$\Rightarrow \bar{A}_I = \bar{A}_{I_1} \cdot \bar{A}'_{I_2} \bar{A}'_{I_3} \cdots \bar{A}'_{In} \longrightarrow ④$$

where $\bar{A}_{I_1} = \frac{\bar{I}_{c_1}}{I_{B_1}}$ = base to Collector Current gain of the first stage

$\bar{A}'_{I_2}, \bar{A}'_{I_3} \cdots \bar{A}'_{In}$ are the Collector to Collector Current gain of 2nd stage, 3rd stage ---- nth stage respectively.

For k^{Th} stage the Collector to Collector Current gain is given by $\bar{A}'_{Ik} = \frac{\bar{I}_{ck}}{\bar{I}_{ck-1}}$

For the same k^{th} stage the base to Collector Current gain is given by $\bar{A}_{Ik} = -\frac{\bar{I}_{ck}}{\bar{I}_{Bk}}$

The relation between $\bar{A}'_{Ik}$ and $\bar{A}_{Ik}$ is given by

$$\bar{A}'_{Ik} = A_{Ik} \frac{R_{c(k-1)}}{R_{c(k-1)} + Z_{ik}} \longrightarrow (5)$$

Eq (5) may be substituted in eq (4) to get the resultant current - gain A_I.

The procedure for calculating the resultant current gain A_I is as follows

i) Find the base to collector current gain of n^{th} stage $\bar{A}_{In}$ i.e the last stage using $\bar{A}_{In} = \frac{-h_{fe}}{1 + h_{oe} R_{Ln}}$

where R_{Ln} = Effective load impedance of n^{th} stage = R_{cn}

ii) Using $\bar{A}_{In}$, R_{Ln} find the input impedance of n^{th} stage

$$Z_{in} = h_{ie} + h_{re} \bar{A}_{In} R_{Ln}$$

iii) Calculate the Effective load impedance $R_{L(n-1)}$ for the $n-1^{th}$ stage $R_{L(n-1)} = R_{c(n-1)} \parallel Z_{i(n)}$

iv) Using $R_{L(n-1)}$ find $\bar{A}_{I(n-1)} = \frac{-h_{fe}}{1 + h_{oe} R_{L(n-1)}}$

v) Using $R_{L(n-1)}$ and $\bar{A}_{I(n-1)}$ find $Z_{i(n-1)}$.

$$Z_{i(n-1)} = h_{ie} + h_{re} A_{I(n-1)} R_{L(n-1)}$$

Proceed in this manner till the first stage

vi) For a particular stage say k^{th} stage the collector to collector current gain $\bar{A}'_{Ik}$ is calculated using

$$\bar{A}'_{Ik} = \bar{A}_{Ik} \cdot \frac{R_{c(k-1)}}{R_{c(k-1)} + Z_{i(k)}}$$

vii) Find the resultant current gain $\bar{A}_I$ for n-stage amplifier using $\bar{A}_I = \bar{A}_{I_1} \cdot \bar{A}'_{I_2} \bar{A}'_{I_3} \cdots \bar{A}'_{In}$.

Power gain ($\bar{A}_p$): The power gain of n-stage cascade amplifier is given by $\bar{A}_p$ = output power of n^{th} stage / Input power of 1^{st} stage

$$\bar{A}_p = \frac{\bar{V}_o \bar{I}_o}{\bar{V}_1 \bar{I}_{B_1}} = \frac{\bar{V}_o(-\bar{I}_{cn})}{\bar{V}_1 \bar{I}_B'}$$

$$\Rightarrow \bar{A}_p = \bar{A}_V \bar{A}_I$$

Substituting $\bar{A}_V = \frac{\bar{A}_I R_{cn}}{z_{i_1}}$

$$\therefore \bar{A}_p = \left(\frac{\bar{A}_I R_{cn}}{z_{i_1}}\right)\bar{A}_I = \frac{(A_I)^2 R_{cn}}{z_{i1}}$$

Input Impedance: By starting from the last stage proceeding towards the first stage, the input impedance can be found out as follows

Find i) $\bar{A}_{I(n)} = \frac{-h_{fe}}{1+h_{oe}R_{Ln}}$ where R_{Ln} = Effective load impedance of n^{th} stage equal to R_{cn}

ii) $\bar{z}_{i(n)} = h_{ie} + h_{re}\bar{A}_{I(n)} R_{Ln}$

iii) $R_{L(n-1)} = R_{c(n-1)} \| z_{i(n)}$, where $R_{L(n-1)}$ is the effective load impedance of $n-1^{th}$ stage.

iv) calculate $\bar{A}_{I(n-1)}$ and $z_{i(n-1)}$ using the above equations. Also find $R_{L(n-2)}$

v) proceed in this manner to find the input impedance of the first stage i.e z_{i1}. The input impedance of the first stage gives the input impedance of the n-stage cascade amplifier.

output impedance:

The output impedance of the complete n-stage cascade amplifier is equal to the output impedance of the nth stage which is calculated starting from 1^{st} stage output impedance.

output admittance of the first stage (transistor) $Y_{o_1} = h_{oe} - \frac{h_{re} h_{fe}}{R_s + h_{ie}}$

$Z_{o_1} = \frac{1}{Y_{o1}}$ = output impedance of the 1st stage transistor.

Parallel combination of Z_{o_1} and R_{c_1} gives the output impedance of the first stage i.e $Z_{os_1} = Z_{o1} \| R_{c_1}$

This Z_{os1} forms the source impedance for the second stage.

Now find Y_{o2} i.e the output admittance of the 2nd stage transistor by replacing R_s with Z_{os1}.

$$Y_{o2} = h_{oe} - \frac{h_{re} h_{fe}}{Z_{os_1} + h_{ie}}$$

$$\Rightarrow \quad Z_{o2} = \frac{1}{Y_{o2}}$$

Now the output impedance of 2nd stage $Z_{os2} = Z_{o2} \| R_{c_2}$.

This Z_{os2} is the source impedance for the third stage.

proceeding in this manner to find the output impedance of the nth stage we get the output impedance of the n-stage cascade amplifier

Distortion in amplifiers:

on application of a sinusoidal signal to the input of the amplifier, the output should be an amplified sinusoidal signal. If the output is not the exact replica of the input wave form, we can say that there is some distortion in the output.

The types of distortion are

1) Non linear distortion 2) Frequency distortion 3) Phase shift distortion

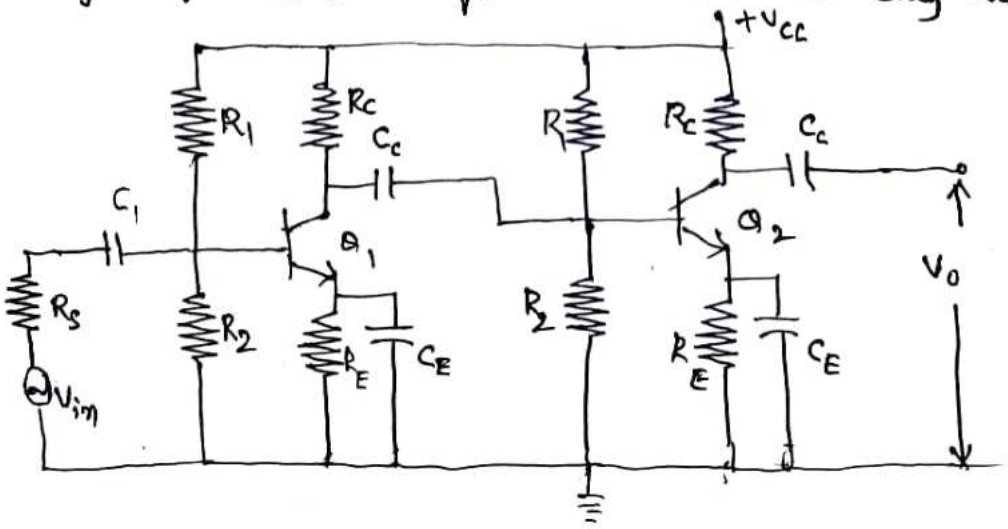
1) Non linear distortion: If the output of an amplifier has some new frequency components that are not present in the input signal, this leads to a distortion called as Non linear distortion. This type of distortion is due to the existence of non linear active devices in the amplifier. This distortion is also called as amplitude distortion.

2) Frequency distortion: This type of distortion exists when the signal components of different frequencies are amplified differently. This distortion may be caused by the internal device capacitances such as transistor capacitance. If the frequency response of an amplifier doesnot have a horizontal line over a range of frequencies, the amplifier is said to have frequency distortion over that range.

3) Phase shift distortion: Phase shift distortion results from unequal phase shifts of the signal at different frequencies. This distortion is due to the fact that the phase shift of the output signal with respect to the input signal, depends on the frequency.

Two stage RC Coupled amplifier using BJT and FET:

A two stage RC coupled CE amplifier with two identical transistors and a common power supply is as shown in figure below. R_C is the load resistor. The resistors R_1, R_2 and R_E are used to provide proper bias. The bypass capacitor C_E prevents the loss of amplification due to negative feed back. The output of the first stage is coupled to the input of the 2nd stage through a coupling capacitor C_c which also serves as the blocking capacitor to block the dc component in the output of the first stage from reaching the input of the 2nd stage and to allow only ac components.



Operation: The ac input signal applied at the base is amplified by the transistor Q_1. It's phase is reversed and the amplified output appears across it's collector load R_c. The output of the first stage across R_c is given as the input to the base of the 2nd stage Q_2 through a coupling capacitor C_c. This signal at the base of Q_2 is further amplified and it's phase is again reversed. Hence the output signal is the amplified replica of the input signal. The output signal is in phase with the input signal because it has been reversed twice.

In the mid frequency range, the gain of the RC coupled amplifier is constant because the coupling and bypass capacitors are as good as short circuits. on both sides of the mid frequency range the gain decreases.

The RC network is wide band in nature. Therefore it gives a wid band frequency response with out peak at any frequency hence it can be used in Audio Frequency range to cover entire frequency band. However the frequency response drops off at very low frequency aswell as at high frequencies.

Advantages of RC coupling:

1) It requires cheap components like resistors and capacitors. Hence it is small, light and inexpensive.
2) It gives a uniform voltage amplification over a wide frequency range from a few KHz to a few MHz
3) Its overall amplification is higher than that of the other couplings.
4) Since it doesnot use any coil or transformer which may pick up unwanted signals. So non linear distortion is very less.

Disadvantages of RC coupling:

1) Due to a large voltage drop across the collector load resistor, the collector works at relatively small voltage. i.e a small voltage from the supply voltage is present at collector.

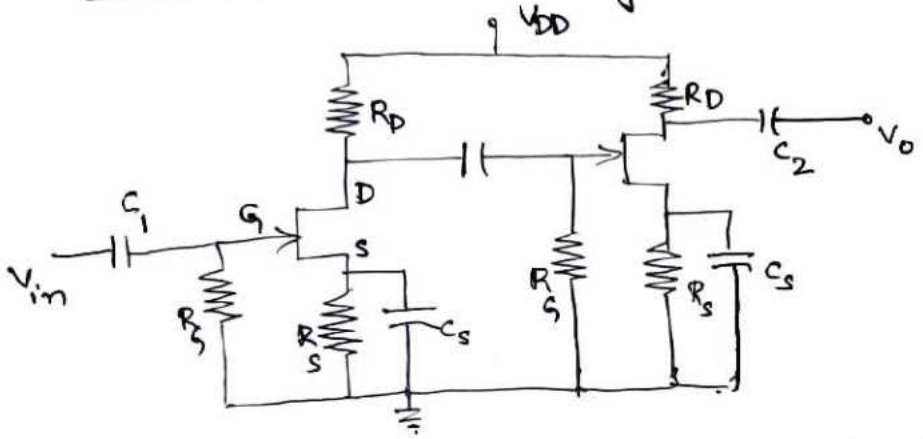
2) The impedance matching is poor as the o/p impedance of RC coupled amplifier is several hundreds of ohms while that of a speaker is only a few ohms. Hence the amount of power transferred to the speaker is reduced.

Applications:

Since the RC coupled amplifier has frequency response over wide range of frequencies, it is extensively used in voltage amplifier, in the initial stages of public address system.

Used in tape recorders, public address systems, radio receivers and TV receivers.

RC coupled Amplifier using FET:



The RC coupled amplifier using FET is as shown in the above figure. R_G is the gate resistor, R_D is the drain resistance. The source resistance R_s is to establish the bias. The bypass capacitor C_s is to prevent the loss of amplification due to negative feedback.

(The remaining explanation is similar to RC coupled amplifier using BJT. Refer that for description).

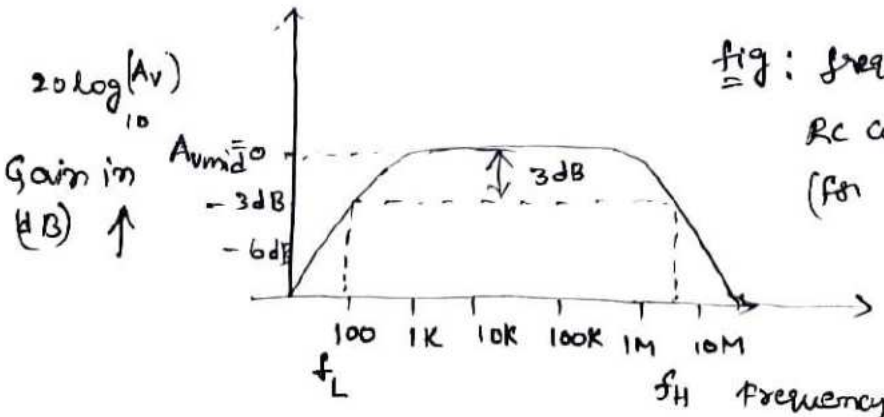


fig: frequency response for RC coupled amplifier (for both BJT & FET)

Transformer Coupled Amplifier:

In a transformer coupled amplifier using transistor, the output of first stage is coupled to the input of the next stage through an impedance matching transformer.

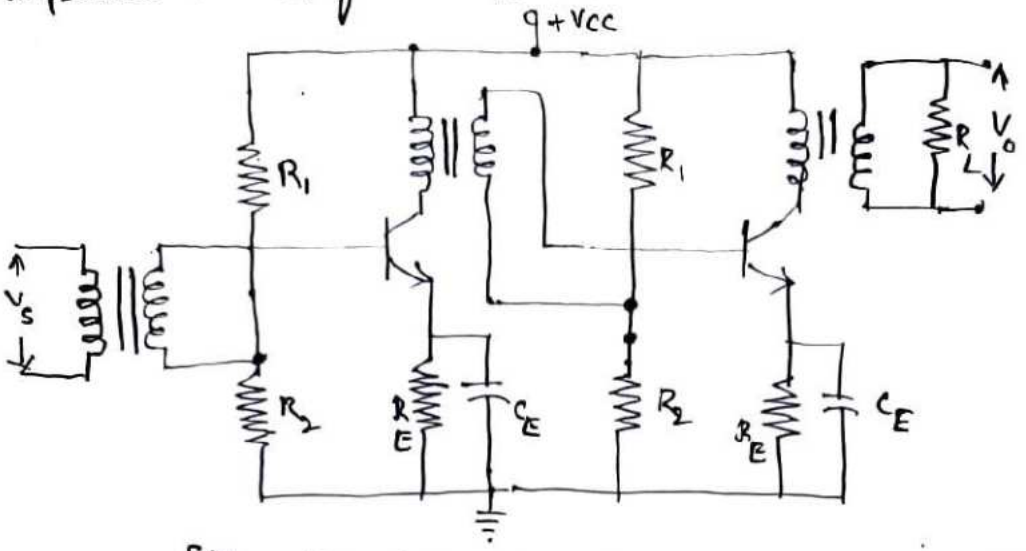


fig: Two stage transformer coupled amplifier using BJT

This type of coupling is used to match the impedance between the output of a stage and the input of another stage.

Usually the output resistance of AF power amplifier is large and it can be matched with a low impedance loudspeaker by using transformer coupling.

The transformer blocks the dc, so it provides the dc isolation between two stages. Therefore it does not affect the Q-point of the next stage.

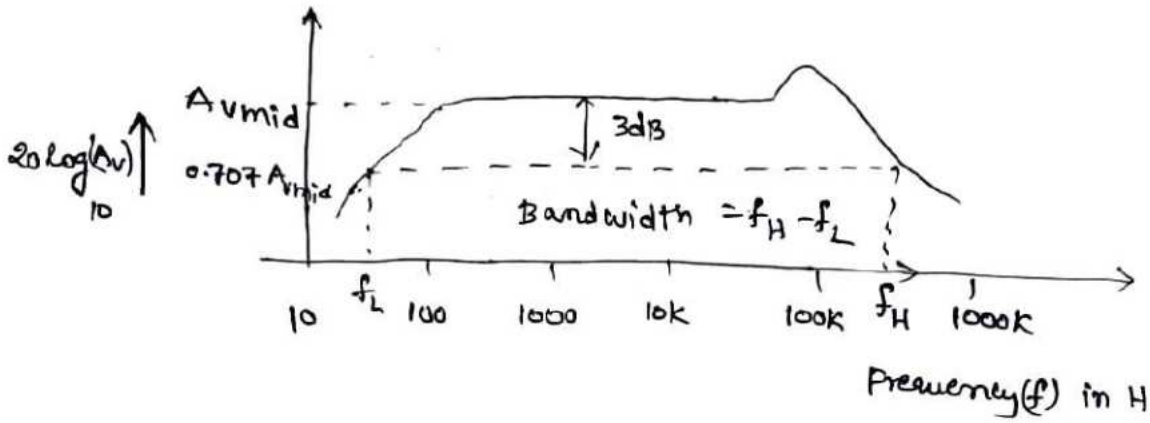
Frequency response of a transformer coupled amplifier is poor in comparison with Rc coupled amplifier. It's leakage inductance and interwinding capacitance of the transformer may give rise resonance at a particular frequency which causes the amplifier to give very high gain at that frequency. By putting shunting capacitors across each winding of the transformer, we can get resonance at any desired RF frequency. Such an amplifier is called as tuned voltage amplifier.

These tuned voltage amplifiers provide high gain at the desired

frequency i.e they amplify highly at selective frequency. For this reason the transformer coupled amplifiers are used in radio and TV receivers for amplifying the RF signals.

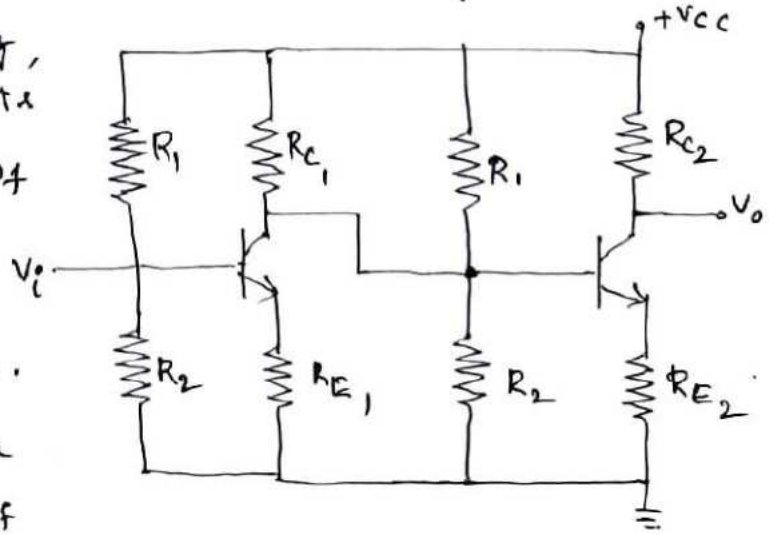
As the d.c. resistance of the transformer winding is very low, almost all the dc supply voltage will appear at the collector terminal of BJT. So, the absense of collector resistor R_c eliminates unnecessary power loss in the resistor unlike RC-Coupled amplifier.

The frequency response of transformer coupled amplifier is as shown in below figure.



Direct Coupled amplifier:

In a direct coupled amplifier the output of the first stage is directly connected, to the input of the next stage as shown in below.



In this direct coupling, it allows the dc components present in the output of the first stage across R_{C_1} to pass to the input of the second stage. This causes a change in the biasing condition of the second stage.

Due to the absence of RC components in a direct coupled amplifier the frequency response is good at low frequencies. But at high frequencies the internal capacitances of the transistor reduce the gain of the amplifier.

The transistor parameters such as V_{BE} and β change with temperature causes a change in V_{CE} and I_C. Because of direct coupling these changes appear at the base of the next stage and hence the output will be getting changed. Such an unwanted change in the output is called drift. Drift is a serious problem in the direct coupled amplifiers.

The frequency response of direct coupled amplifier is as shown in below.

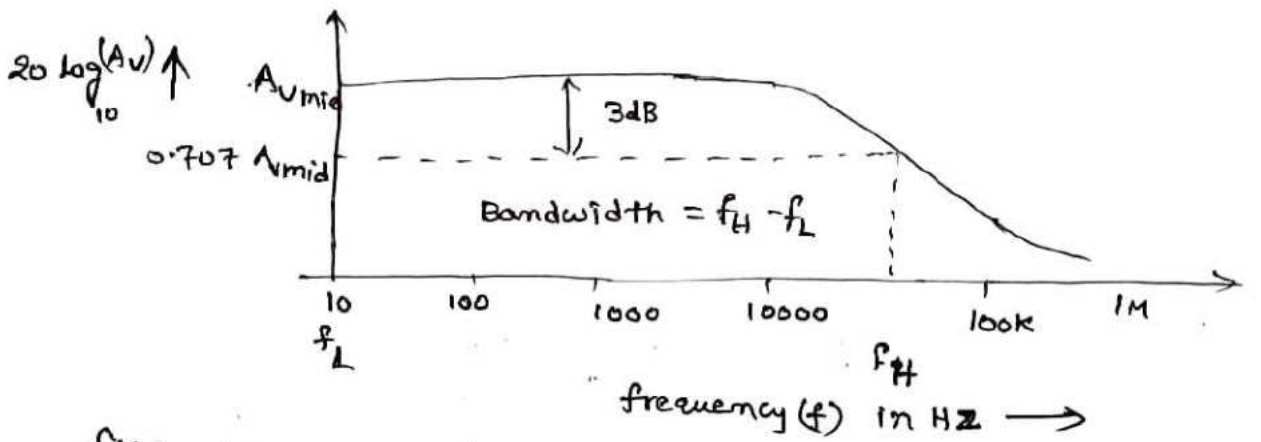


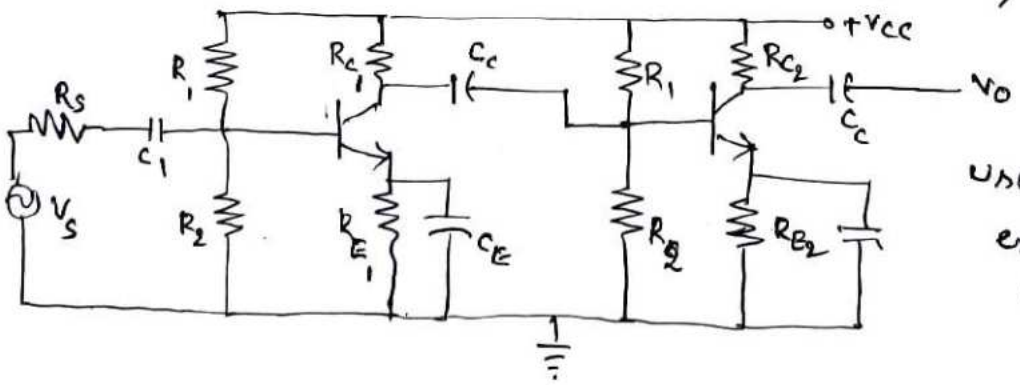
fig: Frequency response of a direct coupled amplifier

Comparison among the RC coupled, transformer coupled and direct coupled amplifiers:

Parameter	RC coupled Amplifier	Transformer coupled Amplifier	Direct Coupled Amplifier
1) Coupling Components	Resistor and Capacitor	Impedance matching transformer	No Coupling network is used.
2) Blocks DC	Yes	Yes	No
3) Frequency response	Frequency response is flat at middle frequencies	Not uniform. Gain is high at resonant frequency.	Flat at middle and low frequencies. Gain decreases at high frequencies.

4) Impedance matching	Is not achieved	Achieved	Not achieved
5) DC amplification	No	No	yes
6) Weight	Light	bulky and heavy	Light
7) Drift	Not present	Not present	present
8) Application	used in record player, tape recorders, radio receivers, TV receivers, and public address system	used in the amplifiers where impedance matching is required. Used in public address system, TV receivers and radio receivers	used in the amplifiers where DC amplification i.e low frequency amplification is required.

Q) Two stage RC coupled CE-CE amplifier has $R_s = 1k\Omega$, $R_{c_1} = 5k\Omega$, $R_{E_1} = 100\Omega$, $R_{c_2} = 4k\Omega$, $R_{E_2} = 330\Omega$ with $R_1 = 200k\Omega$ $R_2 = 20k\Omega$ for first stage and $R_1 = 47k\Omega$ and $R_2 = 4.7k\Omega$ for 2nd stage. Assume $h_{ie} = 1.2k\Omega$, $h_{fe} = 50$, $h_{re} = 2.5 \times 10^{-4}$, $h_{oe} = 25\mu A/V$.



Use approximate and exact analysis both seperately.

Sol

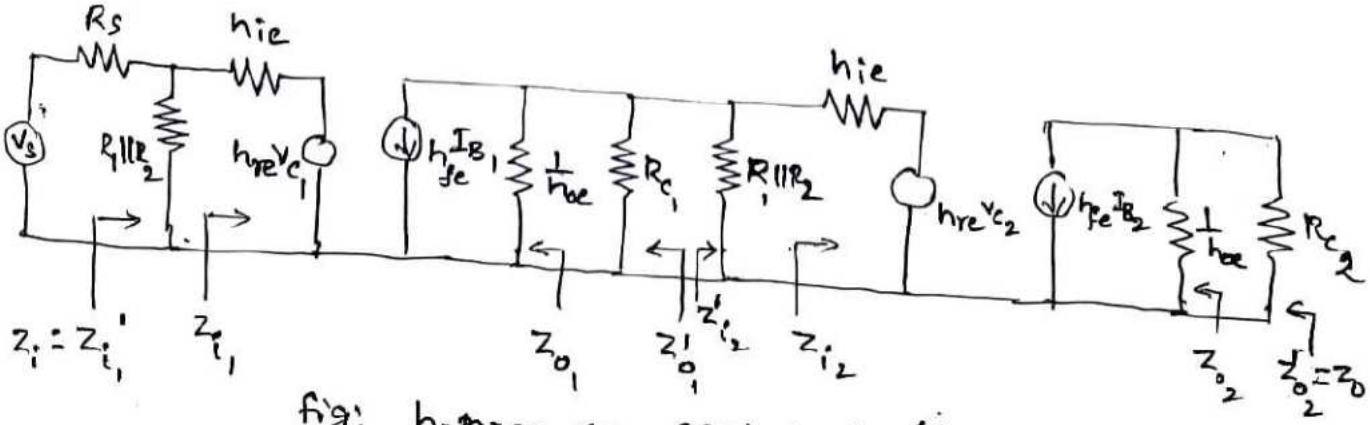


fig: h-parameter equivalent for given circuit

i) Analysis of given CE-CE cascade amplifier using h-parameter approximate analysis:

Analysis of 2nd stage CE amplifier:

$h_{oe} R_{L_2} = h_{oe} R_{C_2} = 25\times10^{-6} \times 4\times10^{3} = 0.1$ we can use approximate model analysis

a) Current gain $A_{I_2} = -h_{fe} = -50$

b) Input resistance $Z_{I_2} = h_{ie} = 1.2k\Omega$ | $Z_{I_2}' = Z_{I_2} \| R_{B_2} = 936.8\Omega$

c) Voltage gain $A_{V_2} = \frac{A_{I_2} R_L}{Z_{I_2}} = \frac{(-50)\times(4\times10^3)}{1.2\times10^3} = -166.67$

Analysis of 1st stage CE amplifier:

$R_{L_1} = R_{C_1} \| R_1 \| R_2 \| Z_{I_2} = 15k \| 47k \| 4.7k \| 1.2k$

$\Rightarrow R_{L_1} = 11.370k\Omega \| 0.9559k\Omega$

$\therefore R_{L_1} = 881.8\Omega$

$h_{oe} R_{L_1} = 25\times10^{-6} \times 881.8 = 0.022 < 0.1$ we can use approximate analysis

a) Current gain $A_{I_1} = -h_{fe} = -50$

b) Input resistance $Z_{I_1} = h_{Ie} = 1.2k\Omega$ and $Z_{I_1}' = Z_{I_1} \| R_{B_1} = 1.125k\Omega$

c) Voltage gain $A_{V_1} = \frac{A_{I_1} R_{L_1}}{Z_{I_1}} = \frac{-50\times881.8}{1.2\times10^3} = -36.74$

overall voltage gain $(A_V) = A_{V_1} \cdot A_{V_2} = (-36.74)(-166.67)$

$\therefore A_V = 6123.45$

overall current gain for two-stage CE-CE amplifier is

$A_I = A_{I_1} A_{I_2}' = -50 \cdot A_{I_2}'$

$A_{I_2}' = \frac{A_{I_2} R_{C_1}'}{R_{C_1}' + Z_{I_2}}$ $\left(\because A_{I_K}' = \frac{A_{I_K} R_{C(K-1)}}{R_{C(K-1)} + Z_{IK}}\right)$

$R_{C_1}' = R_{C_1} \| R_1 \| R_2 = 15K \| 47K \| 4.7K = 15k\Omega \| 4.27K = 3.323k\Omega$

$$\therefore A_{I_2}' = \frac{(-50)(3.323\times10^3)}{(3.323\times10^3)+(1.2\times10^3)} = -36.7344$$

$\therefore$ overall current gain $A_I = A_{I_1} \cdot A_{I_2}' = (-50)\times(-36.7344)$

$$A_I = 1836.72$$

output resistance z_{o_1} for 1st stage $z_{o_1} = \infty$

$$z_{o_1}' = z_{o_1} \| R_{C_1} = \infty \| 15k\Omega = 15k\Omega$$

output resistance z_{o_2} for 2nd stage $z_{o_2} = \infty$

$$z_{o_2}' = z_{o_2} \| R_{C_2} = \infty \| 4k\Omega = 4k\Omega$$

ii) Analysis using Exact h-parameter analysis:

Analysis for 2nd stage CE amplifier:

a) Current gain $A_{I_2} = \frac{-h_{fe}}{1+h_{oe}R_{L_2}} = \frac{-50}{1+(25\times10^{-6})(4\times10^3)} = -45.4545$

b) Input resistance $z_{I_2} = h_{ie} + h_{re}A_{I_2}R_{L_2}$

$$\Rightarrow z_{I_2} = (1.2\times10^3) + (2.5\times10^{-4}) \times (-45.4545)(4\times10^3)$$

$$z_{I_2} = 1.154k\Omega \text{ and } z_{I_2}' = z_{I_2} \| R_{B_2} = 908.599\Omega$$

c) voltage gain $A_{V_2} = \frac{A_{I_2}R_{L_2}}{z_{I_2}} = \frac{(-45.4545)(4\times10^3)}{1.154\times10^3} = -157.554$

Analysis for 1st stage CE amplifier

a) Current gain $A_{I_1} = \frac{-h_{fe}}{1+h_{oe}R_{L_1}}$

$$R_{L_1} = R_{C_1} \| R_1 \| R_2 \| z_{I_2} = 15k \| 47k \| 4.7k \| 1.154k$$

$$\therefore R_{L_1} = 856.268\ \Omega$$

$$\therefore A_{I_1} = \frac{-50}{1+(25\times10^{-6}\times 856.268)} = -48.952$$

b) Input resistance $Z_{I_1} = h_{ie} + h_{re} A_{I_1} R_{L_1}$

$= (1.2 \times 10^3) + (2.5 \times 10^{-4} \times (-48.952) \times 856.268)$

$\therefore Z_{I_1} = 1.189\ k\Omega$

$Z'_{I_1} = R_{B_1} \| Z_{I_1} = (200k \| 20k) \| 1.189k$

$\therefore Z'_{I_1} = 18.18k \| 1.189k = 1.116\ k\Omega$

c) Voltage gain $A_{V_1} = \frac{A_{I_1} R_{L_1}}{Z_{I_1}} = \frac{(-48.952)(856.268)}{1.189 \times 10^3} = -35.253$

overall voltage gain $A_V = A_{V_1} A_{V_2} = (-35.253)(-157.554)$

$\therefore A_V = 5554.25$

overall current gain $A_I = A_{I_1} \cdot A'_{I_2} = -48.952 \cdot A'_{I_2}$

$A'_{I_2} = \frac{A_{I_2} R'_{C_1}}{R'_{C_1} + Z_{i2}} = \frac{-45.4545 R'_{C_1}}{R'_{C_1} + 908.599}$

$R'_{C_1} = R_{C_1} \| R_1 \| R_2 = 15k \| 47k \| 4.7k = 15k \| 4.27k\Omega$

$\therefore R'_{C_1} = 3.323\ k\Omega$

$\therefore A'_{I_2} = \frac{-45.4545 \times (3.323 \times 10^3)}{(3.323 \times 10^3) + 908.599} = -35.6946$

$\therefore A_I = -48.952 \times (-35.6946) = 1747.322$

output resistance $Z_{o_1} = \frac{1}{Y_{o_1}} = \frac{1}{h_{oe} - \frac{h_{re} h_{fe}}{R_s + h_{ie}}}$

$= \frac{1}{25 \times 10^{-6} - \frac{(2.5 \times 10^{-4}) \times 50}{1000 + 1200}}$

$Z_{o_1} = 51.765\ k\Omega$, $Z'_{o_1} = Z_{o_1} \| R_{C_1} = 11.63 k\Omega$

For output resistance Z_{o_2}, the source resistance of second stage is $= Z'_{o_1} \| R_B = Z'_{o_1} \| R_1 \| R_2 = 11.63k \| 47k \| 4.7k$

$\therefore R_{S_2} = 3.124\ k\Omega$

∴ output resistance of second stage transistor

$$Z_{o_2} = \frac{1}{Y_{o_2}} \approx \frac{1}{h_{oe} - \frac{h_r h_f}{Rs_2 + Zi_2}} = \frac{1}{25\times10^{-6} - \frac{2.5\times10^{-4}\times 50}{(3.124\times10^3) + 908.59}}$$

$$= 45.661\ K\Omega$$

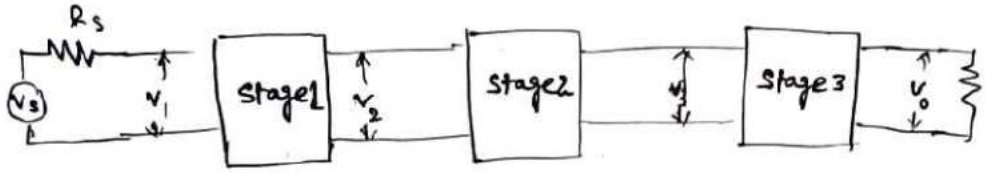
output resistance of second stage amplifier is $Z_{o_2}' = Z_{o_2} \| R_{c_2}$

$$Z_{o_2}' = 45.661\ K\Omega \| 4K\Omega = 3.678\ K\Omega$$

∴ output resistance of overall amplifier = 3.678 KΩ

Problem: A three stage amplifier of cascade has 0.05 V (P-P) input providing 150V (P-P) output. If the voltage gain of the first stage is 20 and input to the third stage is 15V (P-P), find the voltage gain of 2nd and 3rd stages. Find overall gain and the input voltage of 2nd stage

Sol)



Given $V_1 = 0.05V$, $V_0 = 150V(P-P)$

Gain of the third stage $A_{V_3} = ?$, Given $V_2 = 15V(P-P)$

From figure $A_{V_3} = \frac{V_0}{V_2} \Rightarrow A_{V_3} = \frac{150}{15} = 10$

Given $A_{V_1} = 20$, $A_{V_1} = \frac{V_2}{V_1} \Rightarrow V_2 = A_{V_1} \cdot V_1 = 20\times0.05\ V$

$\Rightarrow V_2 = 1V$

$$A_{V_2} = \frac{V_3}{V_2} = \frac{15}{1} = 15$$

∴ overall voltage gain $A_V = A_{V_1} \cdot A_{V_2} \cdot A_{V_3} = 20\times15\times10 = 3000$

∴ Voltage gain of 2nd stage $A_{V_2} = 15$

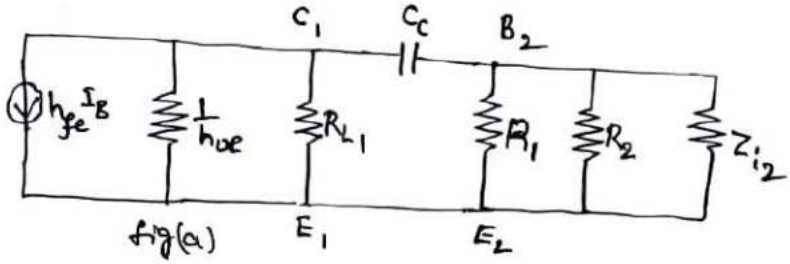
Voltage gain of 3rd stage $A_{V_3} = 10$

Input voltage to 2nd stage = 1V.

Analysis of the effect of Coupling Capacitor on frequency response

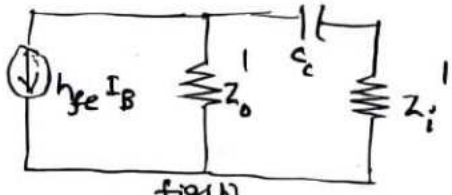
In general emitter bypass capacitance C_E is very large. So it is treated as short circuit for entire range of frequencies.

The output section of 1st stage and the input section of 2nd stage in the h-parameter equivalent circuit is shown in below figure.



fig(a)

This circuit can be further simplified as shown in below figure



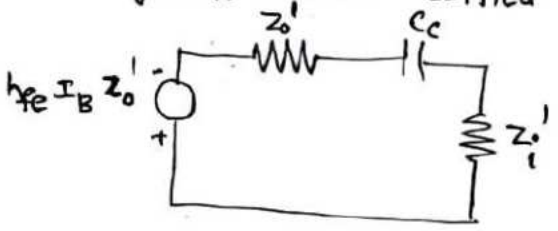
fig(b)

Where $Z_0' = \frac{1}{h_{oe}} \| R_{L1}$

$Z_i' = R_1 \| R_2 \| Z_{i2}$

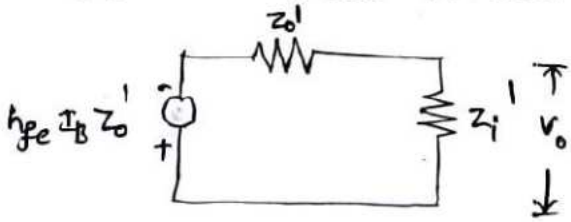
Voltage gain for mid frequency range:

Figure(b) can be modified as shown below.



At mid frequency range the coupling capacitance C_c can be treated as short circuit

∴ The above circuit is redrawn as shown in below by short-circuiting C_c.



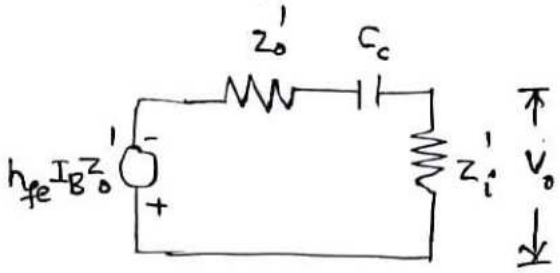
The voltage across Z_i' is $V_o = -\dfrac{h_{fe} I_B Z_0' Z_i'}{Z_0' + Z_i'}$

$$\Rightarrow \frac{V_o}{V_i} = -\frac{h_{fe} I_B Z_0' Z_i'}{(Z_0' + Z_i') V_i}$$

$$\therefore A_{Vmid} = \frac{V_o}{V_i} = -\frac{h_{fe} I_B Z_0' Z_i'}{(Z_0' + Z_i') V_i}$$

Voltage gain at Low frequency range:

At low frequency range the reactance of C_c is large, this large reactance causes voltage drop across the capacitor and resulting the reduction in gain. As signal frequencies decrease, the reactance of the coupling capacitor increases and the gain continues to fall, reducing the output voltage.



From the circuit

$$V_o = \frac{-h_{fe} I_B Z_o' Z_i'}{Z_i' + Z_o' + \frac{1}{j2\pi f C_c}}$$

$$\Rightarrow \frac{V_o}{V_i} = \frac{h_{fe} I_B Z_o' Z_i'}{\left(Z_i' + Z_o' + \frac{1}{j\omega C_c}\right) V_i}$$

$$\Rightarrow A_{VLOW} = \frac{\left(\frac{-h_{fe} I_B Z_o' Z_i'}{Z_o' + Z_i'}\right)\frac{1}{V_i}}{1 + \frac{1}{j\omega C_c (Z_o' + Z_i')}}$$

$$= \frac{A_{V\,mid}}{1 - j\frac{1}{2\pi f C_c (Z_o' + Z_i')}}$$

Let $\frac{1}{2\pi (Z_o' + Z_i') C_c} = f_L$

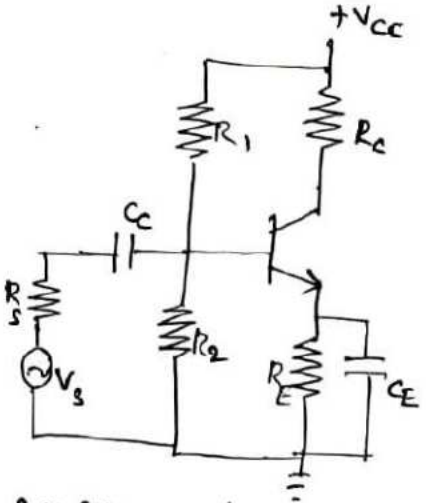
$$\therefore A_{VLOW} = \frac{A_{Vmid}}{1 - j\left(\frac{f_L}{f}\right)} \Rightarrow \left|\frac{A_{VLOW}}{A_{Vmid}}\right| = \frac{1}{\sqrt{1 + \left(\frac{f_L}{f}\right)^2}}$$

at $f = f_L$, $\left|\frac{A_{VLOW}}{A_{Vmid}}\right| = \frac{1}{\sqrt{2}} = 0.707$.

At low frequency $f = f_L$, the voltage gain A_{VLOW} drops to 0.707 times of A_{Vmid} i.e drops to 70.7 % of voltage gain of mid band frequency.

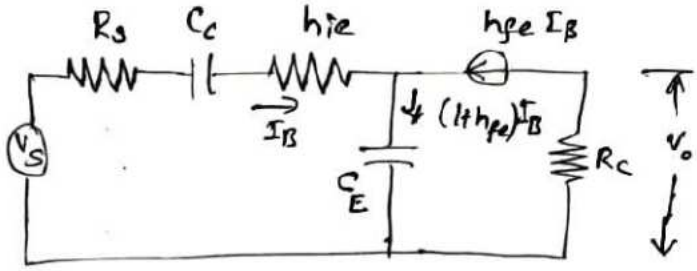
Analysis of the effect of Coupling and bypass capacitances on frequency response at Low frequency range :

Consider a single stage common emitter amplifier as shown below.



fig(a) single stage CE - amplifier

Assume $R_1 \| R_2 \gg R_s$ and R_c is small so that the approximate model shown below is valid.



fig(b) Approximate model for common emitter amplifier shown in fig(a).

The output voltage $V_o = -h_{fe} I_B R_c \longrightarrow (1)$

Applying KVL to the input loop, we get

$$V_s = I_B R_s + I_B\left(\frac{1}{j\omega C_c}\right) + I_B h_{ie} + \frac{I_B(1+h_{fe})}{j\omega C_E} = 0$$

$$V_s = I_B\left(R_s + h_{ie} + \frac{1}{j\omega}\left(\frac{1}{C_c} + \frac{1+h_{fe}}{C_E}\right)\right)$$

$$V_s = I_B\left(R_s + h_{ie} + \frac{1}{j\omega C_1}\right) \text{ where } \frac{1}{C_1} = \frac{1}{C_c} + \frac{1+h_{fe}}{C_E} \longrightarrow (2)$$

From equation (1), equation (2)

$$\frac{V_o}{V_s} = \frac{-h_{fe} R_c}{R_s + h_{ie} + \frac{1}{j\omega C_1}} \longrightarrow (3)$$

At mid band frequency C_1 acts as short circuit. Now eq (3) can be written as

$$A_{V_{mid}} = \frac{V_o}{V_s} = \frac{-h_{fe} R_c}{R_s + h_{ie}} \longrightarrow (4)$$

At low frequency region equation (3) is written as

$$A_{V_{LOW}} = \frac{V_o}{V_s} = \frac{-h_{fe} R_c}{R_s + h_{ie} + \frac{1}{j\omega C_1}}$$

$$\Rightarrow \quad A_{VLOW} = \left(\frac{-h_{fe} R_c}{R_s + h_{ie}}\right) \Big/ \left(1 + \frac{1}{j\omega (R_s + h_{ie}) C_1}\right)$$

$$\Rightarrow \quad A_{VLOW} = \frac{A_{Vmid}}{1 + \frac{1}{j\omega (R_s + h_{ie}) C_1}} = \frac{A_{Vmid}}{1 - \frac{j}{2\pi (R_s + h_{ie}) C_1 f}}$$

$$\Rightarrow \quad A_{VLOW} = \frac{A_{Vmid}}{1 - j\left(\frac{f_L}{f}\right)} \quad \text{where } f_L = \frac{1}{2\pi (R_s + h_{ie}) C_1}$$

$$\text{and } \frac{1}{C_1} = \frac{1}{C_c} + \frac{(1 + h_{fe})}{C_E}$$

$$\therefore \left| A_{VLOW} \right| = \frac{\left| A_{Vmid} \right|}{\sqrt{1 + \left(\frac{f_L}{f}\right)^2}}$$

$$\therefore \left| \frac{A_{VLOW}}{A_{Vmid}} \right| = \frac{1}{\sqrt{1 + \left(\frac{f_L}{f}\right)^2}}$$

$$\text{At } f = f_L, \left| \frac{A_{VLOW}}{A_{Vmid}} \right| = \frac{1}{\sqrt{2}} = 0.707$$

∴ At $f = f_L$, the voltage gain A_{VLOW} drops to 70.7 % of the voltage gain of midband frequency.

Problem: A transistor CE amplifier has $h_{ie} = 600\Omega$, $h_{fe} = 55$, $R_c = 6\,k\Omega$, $R_E = 1.5\,k\Omega$, $C_c = 20\mu F$, $R_s = 1k\Omega$, calculate C_E if $f_L = 50Hz$.

Sol) Given $h_{ie} = 600\Omega$, $h_{fe} = 55$, $R_c = 6k\Omega$, $R_E = 1.5k\Omega$, $C_c = 20\mu F$, $R_s = 1k\Omega$, $f_L = 50Hz$. we know that $f_L = \frac{1}{2\pi (R_s + h_{ie}) C_1}$

$$\Rightarrow 50 = \frac{1}{2\pi C_1 (1 \times 10^3 + 600)} \Rightarrow C_1 = 1.98\,\mu F$$

we know that $\frac{1}{C_1} = \frac{1}{C_c} + \frac{1 + h_{fe}}{C_E} \Rightarrow \frac{1}{1.98 \times 10^{-6}} = \frac{1}{20 \times 10^{-6}} + \frac{1+55}{C_E}$

$$\Rightarrow \frac{56}{C_E} = 455050.5051 \Rightarrow C_E = \frac{56}{455050.5051} = 123.06\,\mu F$$

$$\therefore C_E = 123.06\mu F$$

Effect of Cascading on Gain:

If a number of identical amplifier stages are cascaded using RC coupling, the overall voltage gain is obtained as follows.

Let A_{vmid} = mid band frequency gain of a single stage.

Then the over all mid band frequency gain of cascade amplifier

$$A_{vmid\,(overall)} = A_{vmid} \cdot A_{vmid} \cdot A_{vmid} \cdots A_{vmid} \text{ (n times)}$$

$$\Rightarrow \quad A_{vmid\,(overall)} = (A_{vmid})^n$$

we know that $\left|\frac{A_{VL}}{A_{vmid}}\right| = \frac{1}{\sqrt{1+\left(\frac{f_L}{f}\right)^2}} = \frac{1}{\left[1+\left(\frac{f_L}{f}\right)^2\right]^{1/2}}$

Therefore the overall low frequency gain of the amplifier is

$$\left|\frac{A_{VL}}{A_{vmid}}\right|^n = \frac{1}{\left[1+\left(\frac{f_L}{f}\right)^2\right]^{n/2}}$$

Gain At $f=f_{L(n)}$ i.e at the lower 3dB cutoff frequency of cascade amplifier

$$\left|\frac{A_{VL}}{A_{vmid}}\right|^n = \frac{1}{\left[1+\left(\frac{f_L}{f_{L(n)}}\right)^2\right]^{n/2}} = \frac{1}{\sqrt{2}}$$

Similarly at higher 3dB cutoff frequency $f=f_{H(n)}$ of cascade amplifier the gain is

$$\left|\frac{A_{VH}}{A_{vmid}}\right|^n = \frac{1}{\left[1+\left(\frac{f_{H(n)}}{f_H}\right)^2\right]^{n/2}} = \frac{1}{\sqrt{2}}$$

In General the voltage gain of a cascade amplifier at any frequency over the low frequency range is given by (ie below f_L)

$$A_{VLow\,(overall)} = \frac{(A_{vmid})^n}{\left[1+\left(\frac{f_L}{f}\right)^2\right]^{n/2}}$$

similarly the voltage gain of a multistage amplifier at any frequency over higher frequency range is (i.e above f_H)

$$A_{V\,High\,(overall)} = \frac{(A_{vmid})^n}{\left[1+\left(\frac{f}{f_H}\right)^2\right]^{n/2}}$$

Problem: A multistage amplifier with four identical stages, each of which has a lower cut off frequency 20Hz and upper cut off frequency 20KHz. Calculate the gain of the multistage amplifier at 7.5Hz and at 200KHz. Assume mid band voltage gain of each stage is 10.

Sol) Given $A_{vmid} = 10$, $f_L = 20Hz$, $f_H = 20KHz$, number of stages $n = 4$.

$$A_V(\text{at } f = 7.5Hz) = \frac{(A_{vmid})^n}{\left[1+\left(\frac{f_L}{f}\right)^2\right]^{n/2}}$$

$$= \frac{(10)^4}{\left[1+\left(\frac{20}{7.5}\right)^2\right]^{4/2}}$$

$$= 151.9984$$

$$A_V \text{ at } f = 200KHz) = \frac{(A_{vmid})^n}{\left[1+\left(\frac{f}{f_H}\right)^2\right]^{n/2}} = \frac{10^4}{\left[1+\left(\frac{200\times10^3}{20\times10^3}\right)^2\right]^{4/2}}$$

$$\Rightarrow A_V(\text{at } f = 200KHz) = \underline{0.98029}$$

Effect of Cascading on bandwidth:

The bandwidth of the cascaded amplifier is always less than the bandwidth of a single stage amplifier.

Lower 3dB frequency of cascaded amplifier:

Let the lower 3dB frequency of cascaded amplifier is $f_{L(n)}$, it is the frequency at which the gain falls to $\frac{1}{\sqrt{2}}$ (i.e 3dB) of it's mid band frequency gain

$$\left|\frac{A_{VL}}{A_{vmid}}\right|^n = \left(\frac{1}{\sqrt{1+\left[\frac{f_L}{f_{L(n)}}\right]^2}}\right)^n = \frac{1}{\sqrt{2}}$$

$$\Rightarrow \left[1+\left(\frac{f_L}{f_{L(n)}}\right)^2\right]^{n/2} = 2^{1/2}$$

squaring on both sides $\left[1+\left(\frac{f_L}{f_{L(n)}}\right)^2\right]^n = 2$

$$\Rightarrow 1+\left(\frac{f_L}{f_{L(n)}}\right)^2 = 2^{1/n}$$

$$\Rightarrow \left(\frac{f_L}{f_{L(n)}}\right)^2 = 2^{1/n}-1$$

$$\Rightarrow \frac{f_L}{f_{L(n)}} = \sqrt{2^{1/n}-1}$$

$$\Rightarrow f_{L(n)} = \frac{f_L}{\sqrt{2^{1/n}-1}} \longrightarrow (1)$$

where $f_{L(n)}$ = Lower 3dB cut off frequency of cascade amplifier

f_L = Lower 3dB cut off frequency of a single stage

n = number of stages.

Upper 3dB frequency of cascaded amplifier:

Let the upper 3dB cut off frequency of cascaded amplifier is $f_{H(n)}$, it is the frequency at which the gain falls.

to $\frac{1}{\sqrt{2}}$ (i.e 3dB) of it's mid band frequency voltage gain.

i.e $$\left|\frac{A_{VH}}{A_{Vmid}}\right|^n = \left[\frac{1}{\sqrt{1+\left(\frac{f_{H(n)}}{f_H}\right)^2}}\right]^n = \frac{1}{\sqrt{2}}$$

$$\Rightarrow \left[1+\left(\frac{f_{H(n)}}{f_H}\right)^2\right]^{n/2} = 2^{1/2}$$

squaring on both sides

$$\left[1+\left(\frac{f_{H(n)}}{f_H}\right)^2\right]^n = 2$$

$$\Rightarrow 1+\left(\frac{f_{H(n)}}{f_H}\right)^2 = 2^{1/n}$$

$$\Rightarrow \left(\frac{f_{H(n)}}{f_H}\right)^2 = 2^{1/n} - 1$$

$$\Rightarrow \frac{f_{H(n)}}{f_H} = \sqrt{2^{1/n}-1}$$

$$\therefore f_{H(n)} = f_H\sqrt{2^{1/n}-1} \longrightarrow (2)$$

From equation (1) it is clear that $f_{L(n)}$ is always greater than f_L and from equations (2) $f_{H(n)}$ is always lesser than f_H.

Therefore we can say that the bandwidth of the multistage amplifier is always less than a single stage amplifier.

NOTE: If the stages are not identical f_H can be given as

$$\frac{1}{f_H} = 1.1\sqrt{\frac{1}{f_1^2}+\frac{1}{f_2^2}+\frac{1}{f_3^2}+\cdots+\frac{1}{f_n^2}}$$

Problem: An amplifier consists of three identical stages in cascade, the bandwidth of overall amplifier extends from 20Hz to 20KHz. Calculate the bandwidth of the individual stage.

Sol) Given lower 3dB cut off frequency of multistage amplifier $f_{L(n)} = 20Hz$

Upper 3dB cut off frequency of multistage amplifier $f_{H(n)} = 20KHz$

Let the lower 3dB and upper 3dB cut off frequencies of each identical stage as f_L and f_H. Then

$$f_{L(n)} = \frac{f_L}{\sqrt{2^{1/n}-1}} \Rightarrow f_L = f_{L(n)}\sqrt{2^{1/n}-1}$$ (where $n=3$ given)

$$\Rightarrow f_L = 20\sqrt{2^{1/3}-1}$$

$$\therefore f_L = 10.1964Hz$$

Similarly $f_{H(n)} = f_H\sqrt{2^{1/n}-1}$

$$\Rightarrow f_H = \frac{f_{H(n)}}{\sqrt{2^{1/n}-1}} = \frac{20\times10^3}{\sqrt{2^{1/3}-1}} = 39.229KHz.$$

$\therefore$ Upper cut off frequency of single stage $f_H = 39.229KHz$

Lower cut off frequency of single stage $f_L = 10.1964Hz$

$\therefore$ Bandwidth of individual stage $(BW) = f_H - f_L$

$= 39.229KHz - 10.1964Hz$

$\therefore BW = 39.218KHz$

problem

The bandwidth of the amplifier ranges from 30Hz to 15KHz. Find the frequency range over which A_V is down by 0.5 dB from it's mid band value

Sol)

$$20\log_{10}\left|\frac{A_{VLOW}}{A_{Vmid}}\right| = -0.5$$

$$\log_{10}\left|\frac{A_{VLOW}}{A_{Vmid}}\right| = \frac{-0.5}{20} \Rightarrow \frac{A_{VLOW}}{A_{Vmid}} = 0.944$$

$$\Rightarrow \frac{1}{\sqrt{1+\left(\frac{f_L}{f}\right)^2}} = 0.94406 \qquad \because \frac{A_{VLow}}{A_{Vmid}} = \frac{1}{\sqrt{1+\left(\frac{f_L}{f}\right)^2}}$$

Given $f_L = 30$

$$\Rightarrow \sqrt{1+\left(\frac{f_L}{f}\right)^2} = \frac{1}{0.94406} = 1.05925$$

$$1+\left(\frac{30}{f}\right)^2 = 1.122801$$

$$\Rightarrow \left(\frac{30}{f}\right)^2 = 0.122018$$

$$\Rightarrow f^2 = \frac{900}{0.122018} = 7375.933$$

$$\Rightarrow \therefore f = 85.88\,Hz.$$

$$\left|\frac{A_{VHigh}}{A_{Vmid}}\right| = \frac{1}{\sqrt{1+\left(\frac{f}{f_H}\right)^2}}$$

Given $20 \log_{10}\left|\frac{A_{VHigh}}{A_{Vmid}}\right| = -0.5$

$$\Rightarrow \log_{10}\left|\frac{A_{VHigh}}{A_{Vmid}}\right| = -0.025$$

$$\Rightarrow \left|\frac{A_{VHigh}}{A_{Vmid}}\right| = 10^{-0.025} = 0.94406$$

$$\Rightarrow \frac{1}{\sqrt{1+\left(\frac{f}{f_H}\right)^2}} = 0.94406 \qquad \because \frac{A_{VHigh}}{A_{Vmid}} = \frac{1}{\sqrt{1+\left(\frac{f}{f_H}\right)^2}}$$

Given $f_H = 15\,KHZ$

$$\Rightarrow \sqrt{1+\left(\frac{f}{f_H}\right)^2} = 1.05925$$

$$\Rightarrow 1+\left(\frac{f}{f_H}\right)^2 = 1.122018 \Rightarrow \left(\frac{f}{f_H}\right)^2 = 0.122018$$

$$\Rightarrow \left(\frac{f}{15\times10^3}\right)^2 = 0.122018$$

$\Rightarrow \quad f^2 = 27452376.56$

$\Rightarrow \quad f = 5.239\ kHz$

$\therefore$ The frequency range of amplifier is from 85.88 Hz to 5.239 kHz.

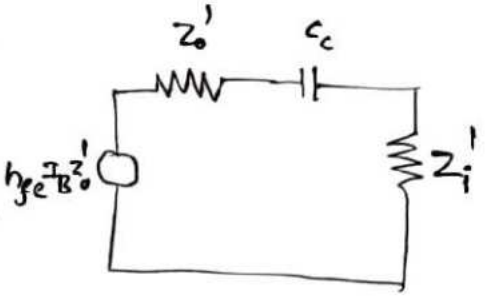
Problem: A single stage coupling capacitors is used between two stages of an amplifier uses a BJT in CE configuration. Parameters are $h_{fe} = 100$, $h_{ie} = 2\ k\Omega$, $R_L = 3\ k\Omega$, $R_1 = 47\ k\Omega$, $R_2 = 4.7\ k\Omega$, $C_c = 5\mu F$. Calculate lower 3dB frequency f_L and calculate the frequency at which voltage gain is down by 12dB from it's mid frequency value. Use approximate analysis.

Sol)

$$Z_o' = Z_o \| R_L$$

for approximate analysis $Z_o = \infty$

$$\therefore Z_o' = R_L = 3k\Omega$$



$$Z_i' = Z_{i_2} \| R_1 \| R_2$$

For approximate analysis $Z_{i_2} = h_{ie} = 2\ k\Omega$

$$\therefore Z_i' = 2k\Omega \| 47k\Omega \| 4.7k\Omega$$

$$Z_i' = 2k\Omega \| 4.272727k\Omega$$

$$Z_i' = 1.3623\ k\Omega$$

Lower 3dB Cut off frequency $(f_L) = \dfrac{1}{2\pi (Z_o' + Z_i')C_c}$

$$f_L = \frac{1}{2\pi (3\times10^3 + 1.3623\times10^3)\times(5\times10^{-6})}$$

$$f_L = 7.2968\ Hz$$

It is given that

$$20 \log_{10} \left| \frac{A_{V\,low}}{A_{V\,mid}} \right| = -12\ dB$$

$$\Rightarrow \log_{10}\left(\frac{A_{VLOW}}{A_{Vmid}}\right) = -0.6$$

$$\Rightarrow \frac{A_{VLOW}}{A_{Vmid}} = 0.25118$$

$$\left[\because \frac{A_{VLOW}}{A_{Vmid}} = \frac{1}{\sqrt{1+\left(\frac{f_L}{f}\right)^2}}\right]$$

$$\frac{1}{\sqrt{1+\left(\frac{f_L}{f}\right)^2}} = 0.25118$$

$$\Rightarrow \sqrt{1+\left(\frac{f_L}{f}\right)^2} = \frac{1}{0.25118} = 3.98107$$

$$1+\left(\frac{f_L}{f}\right)^2 = 15.8489$$

$$\Rightarrow \left(\frac{f_L}{f}\right)^2 = 14.8489$$

From calculation we have got $f_L = 7.2968$ HZ already.

$$\therefore \left(\frac{7.2968}{f}\right)^2 = 14.8489$$

$$\Rightarrow \therefore f = 1.8935 \text{ HZ}.$$

Problem Compute f_H and f_L for a two stage amplifier if $f_{H1} = 3$ KHZ $f_{H2} = 4$ KHZ, $f_{L1} = 300$HZ, $f_{L2} = 600$HZ.

Sol) We know that for multistage amplifier $f_{L(n)} = \frac{f_L}{\sqrt{2^{1/n}-1}}$

$$\Rightarrow f_L = f_{L(n)}\sqrt{2^{1/n}-1}$$

where $f_{L(n)} = \sqrt{f_{L_1}^2 + f_{L_2}^2} = \sqrt{(300)^2+(600)^2} = 670.82$HZ

$$f_{H(n)} = \frac{1}{\sqrt{\frac{1}{f_{H1}^2}+\frac{1}{f_{H_2}^2}}} = \frac{1}{\sqrt{\left(\frac{1}{3\times10^3}\right)^2+\left(\frac{1}{4\times10^3}\right)^2}} = 2400 \text{ HZ}$$

Now $f_H = \frac{f_{H(n)}}{\sqrt{2^{1/n}-1}} = \frac{2400}{\sqrt{2^{1/2}-1}} = 3.729$ KHZ

$$f_L = f_{L(n)}\sqrt{2^{1/n}-1} = 670.82\sqrt{2^{1/2}-1} = 431.71 \text{ HZ}$$

$$\therefore \quad \left| A_{IS} \cdot f_H \right| = \frac{f_T}{1 + 2\pi f_T C_c R_L} \cdot \frac{R_S}{R_S + r_{bb'}}$$

CE - CB Cascode amplifier:

A cascode amplifier consists of CE amplifier stage in series with CB amplifier. This circuit solves the problem of low input impedance of CB amplifier.

The cascode amplifier provides high input impedance, good voltage gain and good frequency response.

The circuit for CE - CB Cascode amplifier is as shown in below.

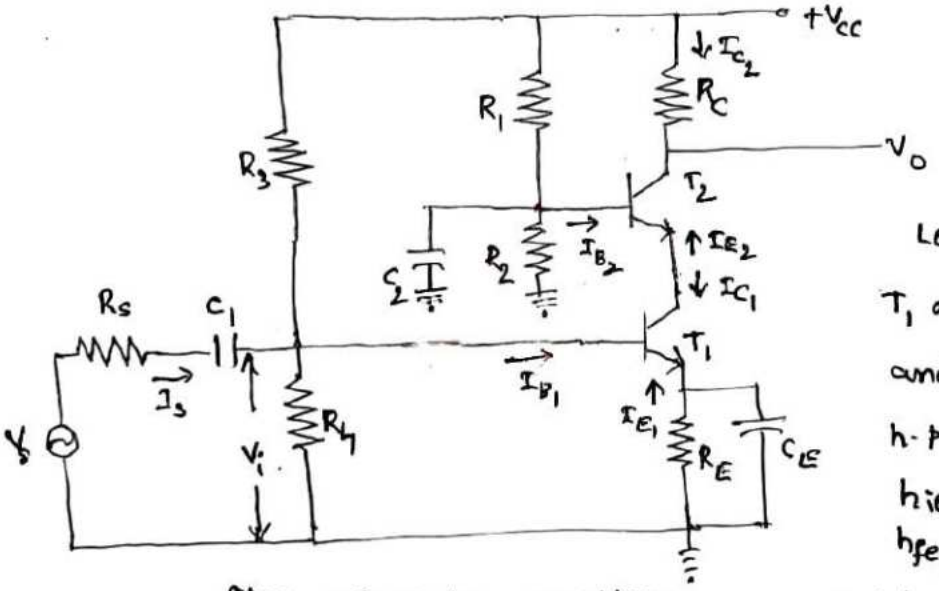


fig: CE-CB Cascode amplifier

Let the transistors T_1 and T_2 are identical and they have same h-parameters. i.e $h_{ie_1} = h_{ie_2} = h_{ie}$, $h_{fe_1} = h_{fe_2} = h_{fe}$, $h_{re_1} = h_{re_2} = h_{re}$ and $h_{oe_1} = h_{oe_2} = h_{oe}$.

In the above circuit the transistor T_1 and it's associated components form the CE amplifier. Similarly the transistor T_2 and it's associated components form the CB amplifier. AC equivalent circuit for Cascode - amplifier is shown below.

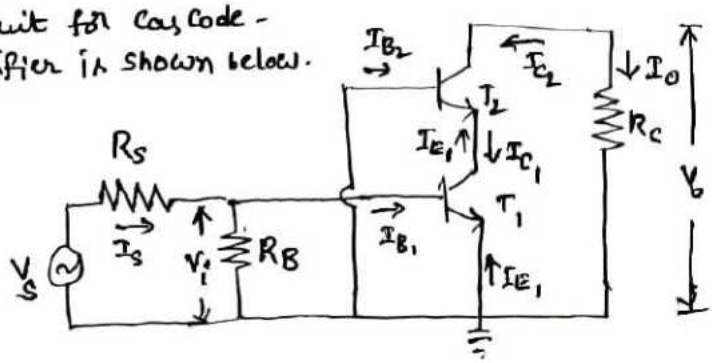


fig: AC equivalent circuit for CE-CB Cascode amplifier.

Here $R_B = R_3 \| R_4$

From the circuit it is clear that $|I_{E_2}| = |I_{C_1}|$ and $|I_{E_1}| = |I_{C_1}|$

The h-parameter equivalent model for CE-CB cascode amplifier using approximate analysis is given below.

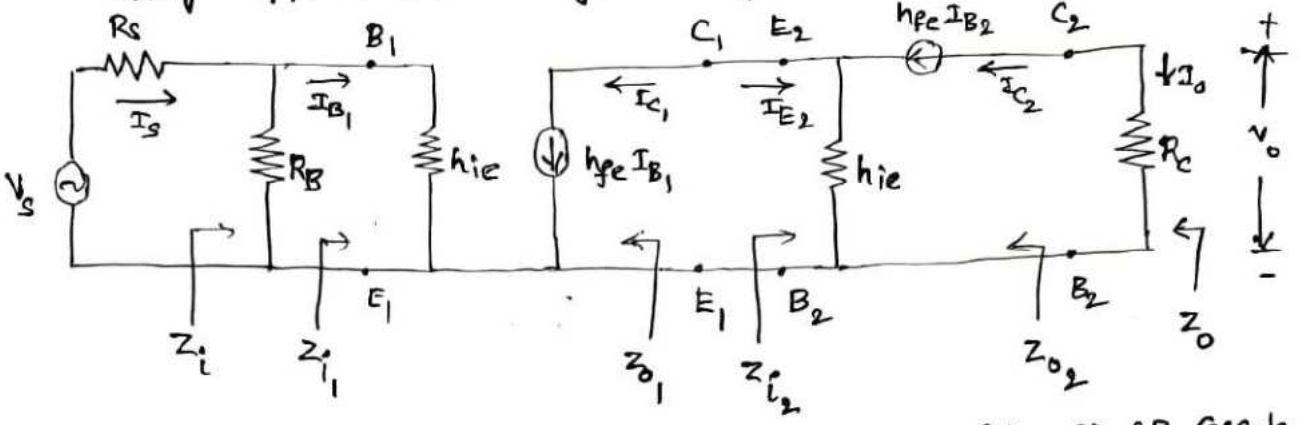


fig: h-parameter equivalent circuit for CE-CB cascode amplifier using approximate model.

Analysis of 2nd stage (CB-amplifier) using approximate model:

a) Current gain $A_{I_2} = -h_{fb} = -\left(\frac{-h_{fe}}{1+h_{fe}}\right) = \frac{h_{fe}}{1+h_{fe}}$

b) Input impedance $Z_{i_2} = h_{ib} = \frac{h_{ie}}{1+h_{fe}}$

c) Voltage gain $A_{V_2} = \frac{A_{I_2} R_{L_2}}{Z_{i_2}} = \frac{A_{I_2} R_C}{Z_{i_2}}$

Analysis of 1st stage (CE-amplifier) using approximate model:

a) Current gain $A_{I_1} = -h_{fe}$

b) Input impedance $Z_{i_1} = h_{ie}$

c) Voltage gain $A_{V_1} = \frac{A_{I_1} R_{L_1}}{Z_{i_1}} = \frac{A_{I_1} Z_{i_2}}{Z_{i_1}}$ $\left(\because \text{from the figure } R_{L_1} = Z_{i_2}\right)$

overall voltage gain $(A_V) = A_{V_1} \cdot A_{V_2}$

overall input impedance $Z_i = Z_{i_1} \| R_B = Z_{i_1} \| R_3 \| R_4$

output impedance for 1st stage $Z_{o_1} = \frac{1}{Y_{o_1}} = \frac{1}{0} = \infty$ $\left(\because \text{for approx. CE model } Y_o = 0\right)$

output impedance for 2nd stage $Z_{o_2} = \frac{1}{Y_{o_2}} = \frac{1}{0} = \infty$ $\left(\because \text{for approx CB model } Y_o = 0\right)$

Overall output impedance $z_o = z_{o_2} \| R_c = \infty \| R_c = R_c$.

Darlington Emitter follower circuit :

A single stage emitter follower (common collector) circuit can give input impedance up to 500 kΩ. The input impedance of the circuit can be improved by direct coupling of two stages of emitter follower amplifier.

The cascaded connection of two emitter followers is called as a Darlington connection.

The Darlington Emitter follower circuit is shown in below circuit.

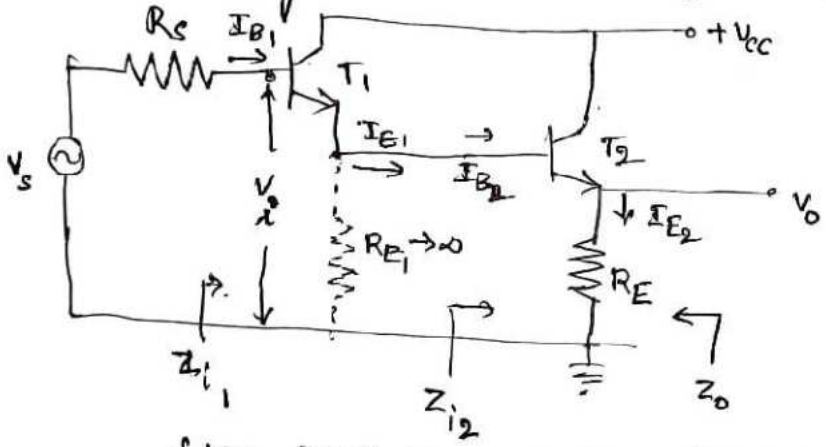


fig: Darlington Emitter follower circuit

In some applications the amplifiers of high input impedance may be required. To achieve larger input impedances darlington connection is used.

Note that the two transistors form a compoite transistor, the input resistance of the 2nd transistor is the load for the first one. Generally the 1st stage has infinite emitter resistance

For second stage assuming $h_{oe} R_E < 0.1$ the analysis is as follows:

Then a) $A_{I_2} = -h_{fc} = 1 + h_{fe}$

b) $Z_{i_2} = h_{ic} + A_I h_{rc} R_E \simeq A_I h_{rc} R_E$

$\therefore Z_{i_2} \simeq (1 + h_{fe}) R_E$ $\quad (h_{rc} \simeq 1)$

c) The voltage gain $A_{V_2} = \dfrac{A_{I_2} R_E}{z_{i2}}$

Analysis of 1st stage:

Load resistance of 1st stage is $R_{L_1} = z_{i2}$

$h_{oe} R_{L_1} = h_{oe} z_{i2} = h_{oe}(1+h_{fe}) R_E > 0.1$ (generally).

So we use exact analysis.

a) Current gain $A_{I_1} = \dfrac{-h_{fc}}{1+h_{oc} R_{L_1}} = \dfrac{1+h_{fe}}{1+h_{oe} z_{i2}} = \dfrac{1+h_{fe}}{1+h_{oe}(1+h_{fe}) R_E}$

$\therefore A_{I_1} = \dfrac{1+h_{fe}}{1+h_{oc} h_{fe} R_E}$ $\left(\because (1+h_{fe}) R_E \simeq h_{fe} R_E\right)$

b) Input impedance $z_{i_1} = h_{ic} + h_{rc} A_{I_1} R_{L_1} = h_{ic} + h_{rc} A_{I_1} z_{i2}$

$\Rightarrow z_{i_1} = h_{ie} + (1)\dfrac{(1+h_{fe})}{1+h_{oe} h_{fe} R_E} \cdot (1+h_{fe}) R_E$

$z_{i_1} \simeq \dfrac{(1+h_{fe})^2 R_E}{1+h_{oe} h_{fe} R_E}$

c) voltage gain $A_{V_1} = \dfrac{A_{I_1} R_{L_1}}{z_{i_1}} = \dfrac{A_{I_1} z_{i2}}{z_{i_1}} = \dfrac{\left(\dfrac{1+h_{fe}}{1+h_{oe} h_{fe} R_E}\right)(1+h_{fe}) R_E}{\dfrac{(1+h_{fe})^2 R_E}{1+h_{oe} h_{fe} R_E}}$

$\Rightarrow A_{V_1} = 1$

overall current Gain $A_I = \dfrac{I_0}{I_{B_1}} = \dfrac{I_{E_2}}{I_{B_1}} = \dfrac{I_{E_2}}{I_{B_2}} \times \dfrac{I_{B_2}}{I_{B_1}}$

$\Rightarrow A_I = A_{I_2} \times \dfrac{I_{E_1}}{I_{B_1}} = A_{I_2} \times A_{I_1}$ $\left(\because I_{B_2} = I_{E_1}\right)$

$\Rightarrow A_I = \dfrac{(1+h_{fe})(1+h_{fe})}{1+h_{oe} h_{fe} R_E}$

$\therefore \boxed{A_I = \dfrac{(1+h_{fe})^2}{1+h_{oe} h_{fe} R_E}}$

Problem A multistage amplifier is constructed by using 4 identical stages, each of which has a lower cut-off frequency of 15Hz and upper cut off frequency of 30KHz. Then

i) Find the lower cutoff frequency and higher cutoff frequency of overall multistage amplifier.

ii) If the mid band voltage gain is of 8.2 for each stage, what will be the approximate voltage gain of multistage-amplifier at 7.5 Hz and 300kHz

Sol) Given $f_L = 15Hz$, $f_H = 30KHz$ (for each stage).

Number of stages $n = 4$

i) Lower cutoff frequency of multistage amplifier of 4-stage is $f_L(n) = \frac{f_L}{\sqrt{2^{1/n}-1}} = \frac{15}{\sqrt{2^{1/4}-1}} = 34.484\,Hz$

Higher cutoff frequency of multistage amplifier $f_{H(n)} = ?$

$$f_H(n) = f_H\sqrt{2^{1/n}-1} = (30\times10^3)\sqrt{2^{1/4}-1}$$

$$\therefore f_H(n) = 13.049\,KHz$$

ii) Given A_{vmid} of each stage is 8.2

i.e $A_{vmid} = 8.2$

The voltage gain at a frequency less than f_L is given by

$$A_{V\,Low\,(overall)} = \frac{(A_{vmid})^n}{\left[1+\left(\frac{f_L}{f}\right)^2\right]^{n/2}} = \frac{(8.2)^4}{\left[1+\left(\frac{15}{7.5}\right)^2\right]^{4/2}} \quad \text{at } f=7.5Hz$$

$$\therefore A_{VLow\,(overall)} \text{ at } f = 7.5Hz = 180.84$$

The voltage gain at a frequency greater than f_H is given by

$$A_{v\,high\,(overall)} = \frac{(A_{vmid})^n}{\left[1+\left(\frac{f}{f_H}\right)^2\right]^{n/2}} = \frac{(8.2)^4}{\left[1+\left(\frac{300\times10^3}{30\times10^3}\right)^2\right]^{4/2}} \quad (\text{at } f = 300KHz)$$

$$\therefore A_{v\,high\,(overall)} = 0.4432$$

UNIT II

FEEDBACK AMPLIFIERS

&

OSCILLATORS

UNIT - II

FEEDBACK AMPLIFIERS

Introduction:

Feedback plays a very important role in electronic circuits and the parameters such as input impedance, current gain, voltage gain, output impedance and bandwidth may be altered considerably by the use of feedback for a given amplifier.

In large signal amplifiers and electronic measuring instruments the major problem of distortion should be avoided as far as possible. And also the gain must be independent of external factors such as variation in dc supply voltage and the values of the circuit components. All this can be achieved with the help of feedback.

A portion of the output signal is taken from the output of the amplifier and is combined with the normal input signal to accomplish the feed-back for an amplifier.

Classification of Basic amplifiers:

The basic amplifiers are classified into four categories as voltage amplifier, current amplifier, transconductance amplifier and trans resistance amplifier based on the magnitudes of input and output resistances of an amplifier with respect to the source and load resistances. These basic amplifiers are used in feed-back amplifiers.

Voltage Amplifier:

The figure shows a thevenin's equivalent circuit of a voltage-amplifier.

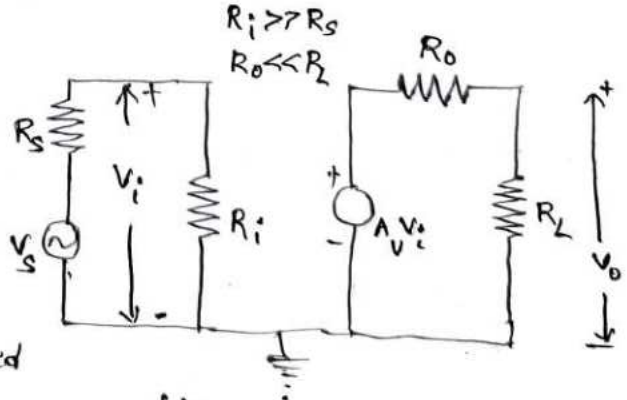


fig: voltage amplifier

An Ideal voltage amplifier is defined as an amplifier which provides the output voltage proportional to the input voltage and the proportionality factor doesnot depend on the magnitude of source and load resistances. An ideal voltage amplifier has

$V_o \simeq A_v V_s$

infinite input resistance (R_i) and zero output resistance (R_o). But a practical voltage amplifier has $R_i >> R_s$ and $R_o << R_L$.

The output voltage $V_o \simeq A_v V_i \simeq A_v V_s$ where A_v is the open circuit voltage gain with $R_L = \infty$.

Current Amplifier:

Figure shows the Norton's equivalent circuit for current amplifier. An ideal current amplifier is defined as an amplifier which provides the output current proportional to the input current and the proportionality factor is independent of R_s and R_L.

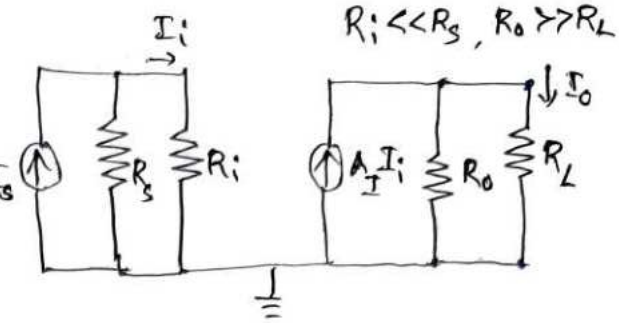


fig: Current amplifier

$I_o \simeq A_I I_s$

An ideal current amplifier has zero input resistance (R_i) and infinite output resistance (R_o). But practical current-amplifier has $R_i << R_s$ and $R_o >> R_L$.

The output current $I_o \simeq A_I \cdot I_i$, where A_I is the short circuit current gain with $R_L = 0$.

Transconductance amplifier:

Figure shows the transconductance amplifier in which the input circuit is thevenin and output circuit is norton.

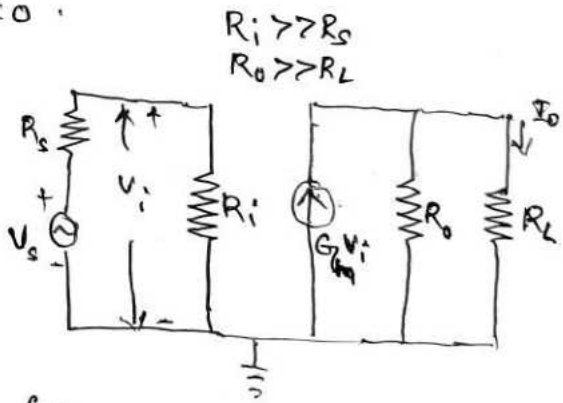


fig: Transconductance Amplifier

$I_o \simeq G_m V_s$

An Ideal transconductance amplifier is defined as an amplifier in which the output current is proportional to the input voltage and the proportionality factor is independent of R_s and R_L.

An ideal transconductance amplifier has $R_i = \infty$ and $R_o = \infty$. But practical transconductance amplifier has $R_i >> R_s$, $R_o >> R_L$.

The output current $I_o \simeq G_m V_i$, where G_m is short circuit transconductance with $R_L = 0$

Transresistance Amplifier:

Figure shows the transresistance amplifier in which the input is Norton and output is thevenin.

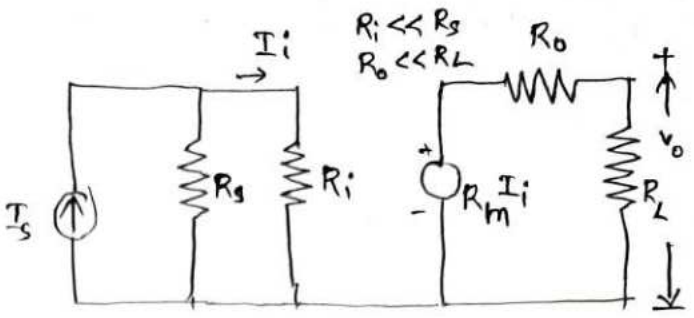


fig: Transresistance amplifier

$V_o \simeq R_m I_s$

An Ideal transresistance amplifier is defined as an amplifier the output voltage is proportional to the input current and proportionality factor is independent of the values of R_s and R_L.

For an ideal transresistance amplifier $R_i = 0$ and $R_o = 0$. But in practical transresistance amplifier $R_i \ll R_s$ and $R_o \ll R_L$.

The output voltage $V_o = R_m \cdot I_i$ where R_m is opencircuit transfer resistance with $R_L = \infty$.

Basic Concept of feedback:

The block diagram of an amplifier with feedback is shown in below figure

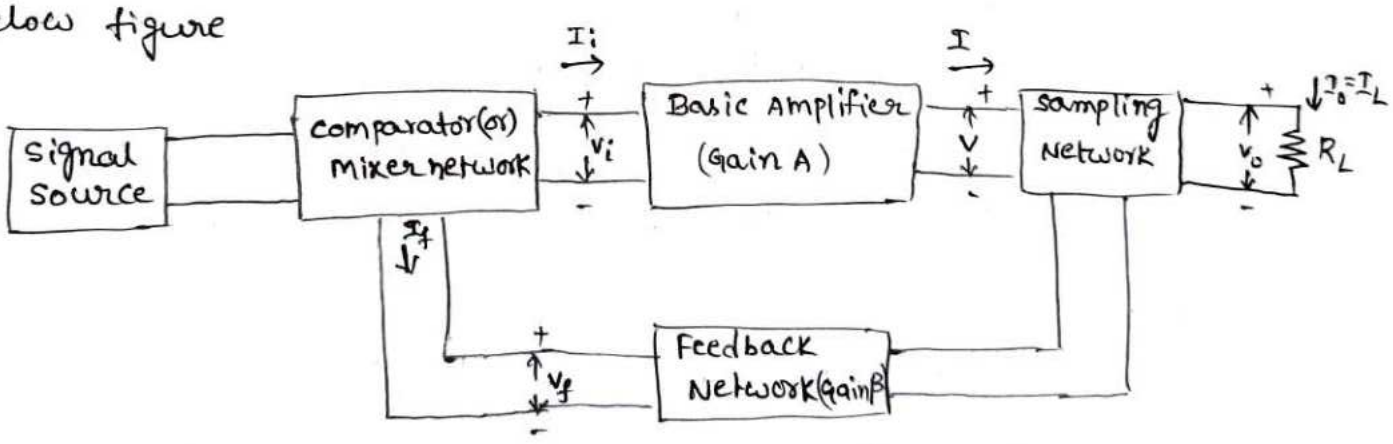


fig: Blockdiagram of an amplifier with feedback

In a feedback amplifier a basic amplifier is used that can be a voltage amplifier (or) a current amplifier (or) transconductance (or) transresistance amplifier. In each one of these circuits we may sample the output voltage (or) output current by means of a suitable sampling network which is of two types, namely, voltage sampler and current sampler. and apply the sampled signal to the

feed back network. The output of the feedback network is combined with the source signal through a mixer and fed to the basic amplifier.

Mixers are also known as comparators which are of two types series mixer and shunt mixer.

In the block diagram shown above we have

A = Gain of the basic amplifier = $\frac{V}{V_i}$

β = feed back ratio (or) reverse transmission factor

$= \frac{V_f}{V_o}$

A_f = gain of the feed back amplifier = $\frac{V_o}{V_s}$

V_s = signal voltage from the source.

V_f = feedback signal voltage.

The signal source in a feed back amplifier can be either a signal voltage V_s in series with a resistor R_s (or) a signal current I_s in parallel with a resistor R_s.

The feedback network may contain resistors, capacitors and inductors. Most often it is simply a resistive configuration.

If sampling network is a voltage sampler, the output voltage is sampled by connecting the feedback network in shunt across the o/p. If it is a current sampler the output current is sampled by connecting the o/p to feedback network in series.

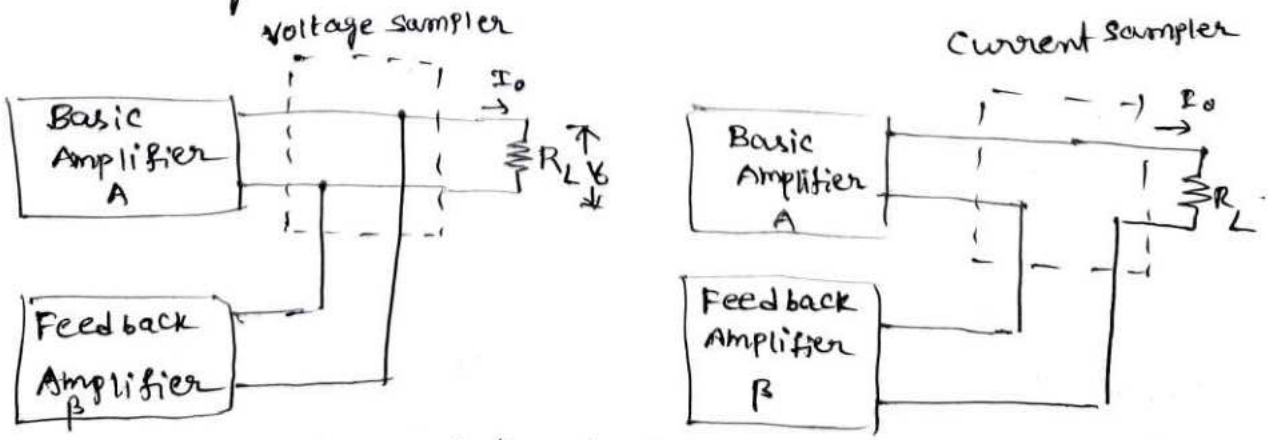


Fig:- Feedback Connections at the o/p of a basic amplifier, sampler o/p.

Mixer (or) comparator network is used for combining the feedback signal with the input signal. There are two types of mixer networks series mixer and shunt mixer as shown in below.

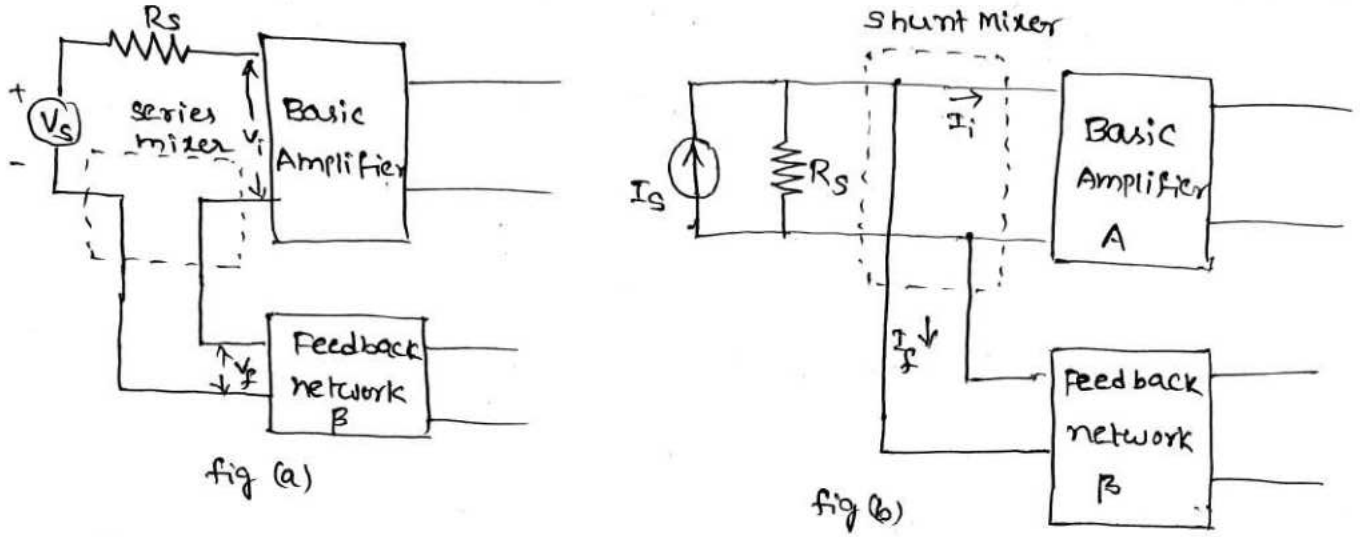


fig: Feedback connections at the input of the basic amplifier
fig(a) using series mixing fig(b) using shunt mixing

Transfer ratio(or) Gain:

The ratio of the output signal to the input signal of a basic amplifier is called as transfer ratio denoted as 'A'.

The transfer ratio V/V_i is the voltage gain denoted by A_V. Similarly the transfer ratio $\frac{I}{I_i}$ is the current gain denoted by A_I.

The transfer ratio $\frac{I}{V_i}$ is the trans conductance denoted by G_m. and the transfer ratio $\frac{V}{I_i}$ is the transresistance R_M.

Generally each of these four A_V, A_I, G_M and R_M are referred as the transfer gain of the basic amplifier without feedback and we use the symbol A to represent any one of these quantities.

The symbol A_f is defined as the ratio of the output signal to the input signal of the amplifier and is called as transfer gain of the amplifier with feedback. Hence A_f is used to represent any one of the four ratios $\frac{V_o}{V_s} = A_{Vf}$, $\frac{I_o}{I_s} = A_{If}$, $\frac{I_o}{V_s} = G_{mf}$, $\frac{V_o}{I_s} = R_{mf}$

Schematic representation (or) the general structure of a feedback amplifier:

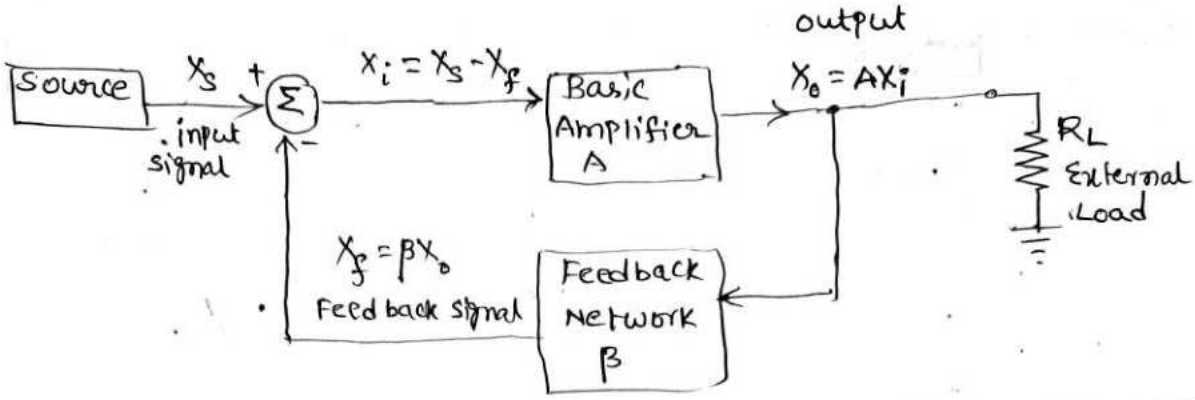


fig: Schematic representation of a single loop feed back amplifier.

The above figure shows the schematic representation of a feedback amplifier. Here X represents either voltage or current signals. when the feedback signal(X_f) and input signal (X_s) are out of phase that feedback is called negative feedback and if the feed back signal (X_f) and input signal (X_s) are in phase, that feedback is called as positive feedback.

Negative feed back is also called as degenerative feedback where as positive feed back is also called as regenerative feedback.

Positive feed back:

Positive feed back is also known as regenerative feedback. If the feedback signal (X_f) is in phase with the input signal X_s then that feed back is called as positive feedback. In this case, the positive feedback causes the input of the basic amplifier(X_i) to be increased, which causes the output (X_o) to increase.

The gain of amplifier with positive feed back is

$$A_f = \frac{X_o}{X_s} = \frac{X_o}{X_i - X_f}$$

$$\Rightarrow A_f = \frac{1}{\left(\frac{X_i}{X_o}\right) - \left(\frac{X_f}{X_o}\right)} = \frac{1}{\left(\frac{1}{A}\right) - \beta} = \frac{A}{1 - A\beta}$$

$$\therefore A_f = \frac{A}{1 - A\beta}$$

Here $|A_f| > |A|$. The product of open loop gain and the feed back factor (β), is called as loop gain i.e loop gain = $A\beta$

If $|A\beta| = 1$ then $A_f = \infty$. Hence the gain of the amplifier with positive feedback is infinite and the amplifier gives an ac signal with out ac input signal. Drawbacks of positive feedback is the positive feedback increases the instability of an amplifier, reduces the bandwidth and increases the distortion and noise.

The positive feedback is used in oscillators.

Negative feedback:

If the feedback signal (X_f) is out of phase with the input signal (X_s) then that feedback is called as negative feedback.

The negative feedback causes the input of the basic amplifier (X_i) to be decreased causing the output (X_o) to be decreased.

Negative feedback is also called as degenerat feedback.

The gain of the amplifier with negative feedback is

$$A_f = \frac{X_o}{X_s} = \frac{X_o}{X_i + X_f}$$

$$\Rightarrow A_f = \frac{1}{\frac{X_i}{X_o} + \frac{X_f}{X_o}} = \frac{1}{\frac{1}{A} + \beta} = \frac{A}{1 + A\beta}$$

$$\therefore A_f = \frac{A}{1 + A\beta}$$

Here $|A_f|$ is less than $|A|$. If $|A\beta| >> 1$ then $A_f = \frac{1}{\beta}$ where β is feedback ratio. Then the gain A_f depends completely on feedback network.

If the feedback network contains only passive elements, the gain of the amplifier with negative feedback will be stable.

Advantages of negative feedback: (characteristics of negative feedback)

The stabilization of the operating point of a transistor amplifier is accomplished by using negative feedback with respect to the changes in dc supply voltage and the operating point is kept constant in the case of change in temperature or a change in h_{fe}

(or) β of a transistor.

Negative feedback is also used to improve the performance of an amplifier i.e frequency response is improved with negative feedback.

Negative feedback always helps to increase the bandwidth, decrease distortion and noise, modify the input and output resistances as desired.

All the above advantages are derived at an expense of reduction in voltage gain. But the amplifier with negative feedback provides a stabilised voltage gain.

Classification of feedback amplifiers (or) Feedback topologies:

Based on the type of sampling at output side and the type of mixing to the input side, feedback amplifiers are classified into four topologies. They are

1) Voltage series feedback (or) series shunt feedback
2) Current series feedback (or) series series feedback
3) Current shunt feedback (or) shunt series feedback
4) Voltage shunt feedback (or) shunt shunt feedback

The feedback amplifier topologies are given below.

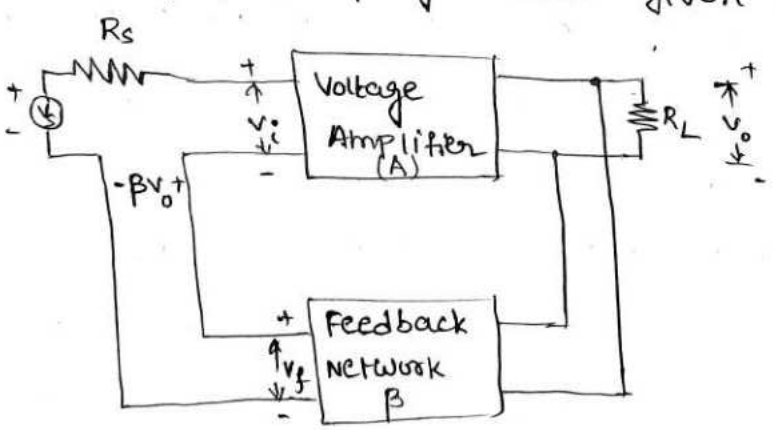


fig: Voltage series feedback Topology

(or) Voltage amplifier with Voltage series feedback

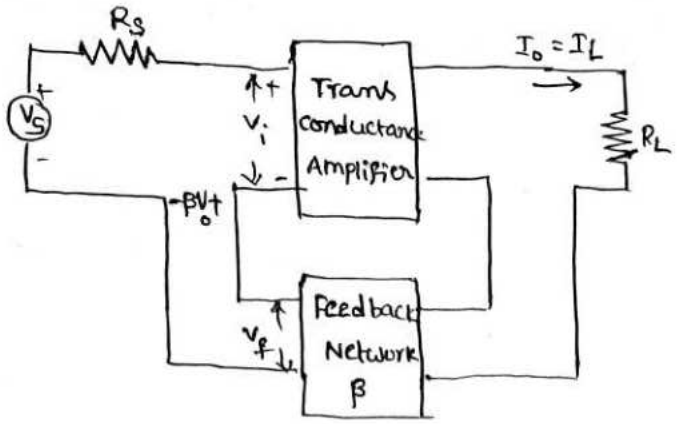


fig: Current series feedback (or) Transconductance amplifier with current series feed back.

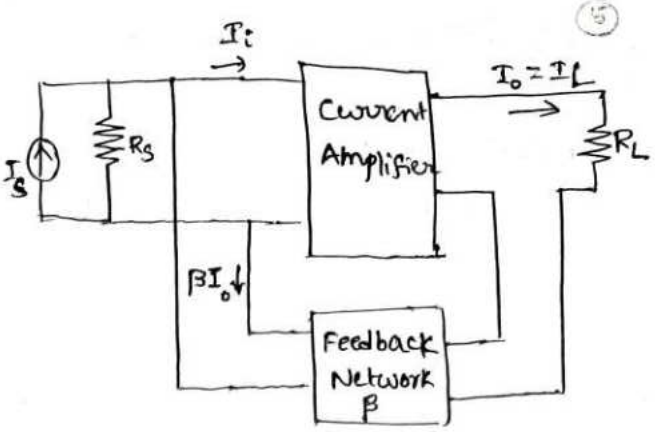


fig: current shunt feedback (or) current amplifier with current shunt - feedback

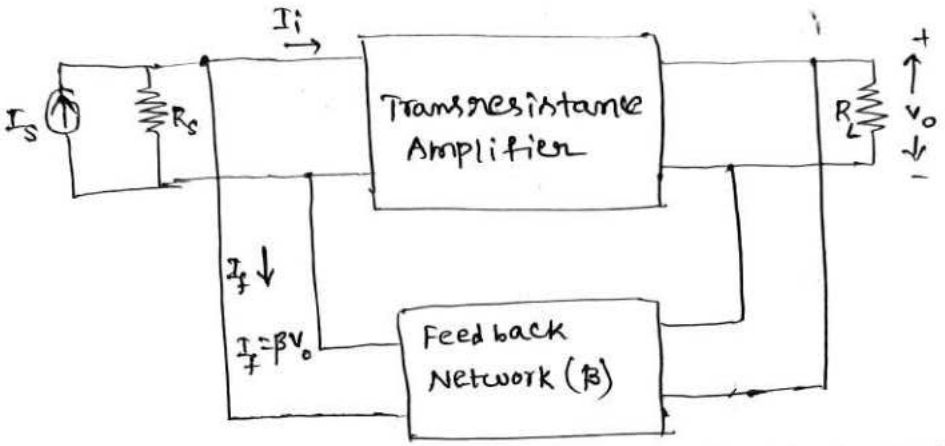


fig: Transresistance amplifier with feed back network i.e Voltage shunt feed back

Let the input signal as X_s, the output signal X_o, the feedback signal X_f and the input of the basic amplifier is X_i. These signals and the corresponding ratios A and β are listed below.

Signal (or) ratio	Voltage series feed back	Current series feed back	Current shunt feedback	Voltage shunt feed back
X_o	Voltage	Current	Current	Voltage
X_s, X_f and X_i	Voltage	Voltage	Current	Current
A	A_V	G_M	A_I	R_M
β	$\frac{V_f}{V_o}$	$\frac{V_f}{I_o}$	$\frac{I_f}{I_o}$	$\frac{I_f}{V_o}$

Characteristics of negative feed back amplifiers

1) Stability of gain (or) Desensitization :

The gain of the amplifiers is not constant in general as it depends on the factors such as temperature, aging of the components and temperature dependent parameters. This lack of stability can be reduced by introducing negative feed back.

we know that the expression for gain with feedback

$$A_f = \frac{A}{1+A\beta} \longrightarrow (1)$$

differentiating A_f with respect to A.

$$\frac{dA_f}{dA} = \frac{(1+A\beta).(1) - A.(\beta)}{(1+A\beta)^2}$$

$$\frac{dA_f}{dA} = \frac{1}{(1+A\beta)^2}$$

multiplying both sides with $\frac{1}{A_f}$ we get

$$\frac{dA_f}{dA} \cdot \frac{1}{A_f} = \frac{1}{(1+A\beta)^2} \cdot \frac{1}{A_f}$$

$$\frac{dA_f}{dA} \cdot \frac{1}{A_f} = \frac{1}{(1+A\beta)^2} \cdot \frac{1}{\frac{A}{(1+A\beta)}}$$

$$\frac{dA_f}{A_f} = \frac{dA}{A} \cdot \frac{1}{(1+A\beta)}$$

$$\Rightarrow \left(\frac{dA_f}{A_f}\right) \Big/ \left(\frac{dA}{A}\right) = \frac{1}{1+A\beta}$$

$$\therefore S = \frac{1}{1+A\beta} \longrightarrow (2)$$

The fractional change in amplification with feedback is divided by the fractional change in amplification with out feedback is called as sensitivity of the transfer gain denoted by S

The reciprocal of sensitivity is known as desensitivity denoted by D. i.e $D = \frac{1}{S} = \frac{1}{(1/1+A\beta)} = 1+A\beta$ → (3)

From equation (1) and (2) $A_f = \frac{A}{D}$

In equation (1) if $\beta A >> 1$ then $A_f = \frac{A}{1+\beta A} \simeq \frac{A}{\beta A} \simeq \frac{1}{\beta}$

Thus the gain A_f is made to depend entirely on feedback network. If the feed back network contains only passive elements the improvement in stability is achieved.

Then the voltagain $A_{Vf} \simeq 1/\beta$ for voltage series feed back, Transconductance $G_{mf} \simeq \frac{1}{\beta}$ for current series feed back, the current gain $A_{If} \simeq \frac{1}{\beta}$ for a current shunt feed back and the trans resistance $R_{mf} \simeq \frac{1}{\beta}$ for a voltage shunt feed back is achieved.

2) Extension of bandwidth :

we know that the gain of the amplifier with negative feed back is given as $A_f = \frac{A}{1+A\beta}$ → (1)

Then we can write $A_{fmid} = \frac{A_{mid}}{1+A_{mid}\beta}$ → (2)

$A_{flow} = \frac{A_{low}}{1+A_{Low}\beta}$ → (3)

$A_{fhigh} = \frac{A_{high}}{1+A_{high}\beta}$ → (4)

The ebbect of negative feedback on lower cut-off and upper-cut off frequencies of the amplifier is analysed here.

Lower cut-off frequency : (f_{Lf})

we know that the relation between the gain at lower-cut off frequency and the gain at mid band frequency of an amplifier is given as $A_{low} = (A_{mid}) / \left[1 - j\left(\frac{f_L}{f}\right)\right]$ → (5)

Substitute equation (5) in equation (3) we get

$$A_{f\,low} = \frac{(A_{mid})/(1 - j\frac{f_L}{f})}{1 + \left[A_{mid}/(1 - j\frac{f_L}{f})\right]\cdot\beta}$$

$$= \frac{A_{mid}}{1 - j\frac{f_L}{f} + A_{mid}\cdot\beta}$$

$$\therefore = \frac{A_{mid}}{(1 + A_{mid}\beta) - j\frac{f_L}{f}}$$

Dividing the numerator and the denominator with $\frac{1}{1 + A_{mid}\beta}$ we get

$$A_{f\,low} = \frac{\frac{A_{mid}}{(1 + A_{mid}\cdot\beta)}}{1 - j\left(\frac{f_L}{1 + A_{mid}\beta}\right)\frac{1}{f}}$$

$$A_{f\,low} = \frac{A_{f\,mid}}{1 - j\left(\frac{f_{Lf}}{f}\right)} \qquad \left(\text{since } A_{f\,mid} = \frac{A_{mid}}{1 + A_{mid}\beta}, \text{ let } f_{Lf} = \frac{f_L}{1 + A_{mid}\beta}\right)$$

where $f_{Lf} = \frac{f_L}{1 + A_{mid}\beta}$ is the lower cut off frequency with feed back.

From this equation of f_{Lf} it is clear that the lower cutoff frequency of an amplifier with feed back (f_{Lf}) is lesser than that of the lower cut off frequency of an amplifier without feed-back (f_L) by a factor $(1 + A_{mid}\beta)$. Thus by introducing negative feedback, low frequency response of an amplifier is improved.

Higher Cut-off frequency (f_{Hf}):

We know that $A_{high} = \frac{A_{mid}}{1 + j\left(\frac{f}{f_H}\right)}$ ⟶ (6)

Substituting equation (6) in equation (4) we get

$$A_{f\,high} = \left[\frac{A_{mid}}{1 + j\left(\frac{f}{f_H}\right)}\right] \Big/ \left[1 + \left(\frac{A_{mid}}{1 + j\left(\frac{f}{f_H}\right)}\right)\cdot\beta\right]$$

$$\Rightarrow A_{f\,high} = \frac{A_{mid}}{1 + j\frac{f}{f_H} + A_{mid}\beta}$$

$$\Rightarrow A_{f\,high} = \frac{A_{mid}}{(1 + A_{mid}\beta) + j\frac{f}{f_H}}$$

Dividing the numerator and denominator of RHS with $1 + A_{mid}\beta$ we get

$$A_{f\,high} = \frac{\frac{A_{mid}}{1 + A_{mid}\beta}}{1 + j\frac{f}{f_H(1 + A_{mid}\beta)}} = \frac{A_{f\,mid}}{1 + j\frac{f}{f_{Hf}}}$$

where $A_{f\,mid} = \frac{A_{mid}}{1 + A_{mid}\beta}$ and $f_{Hf} = f_H(1 + A_{mid}\beta)$

f_{Hf} is the higher cut off frequency of an amplifier with feedback.

From the equation of f_{Hf} it is clear that upper cut off frequency of an amplifier with feedback (f_{Hf}) is greater than the upper cut off frequency of an amplifier without feedback (f_H) by a factor $1 + A_{mid}\beta$. Therefore by introducing negative feedback high frequency response of the amplifier is improved.

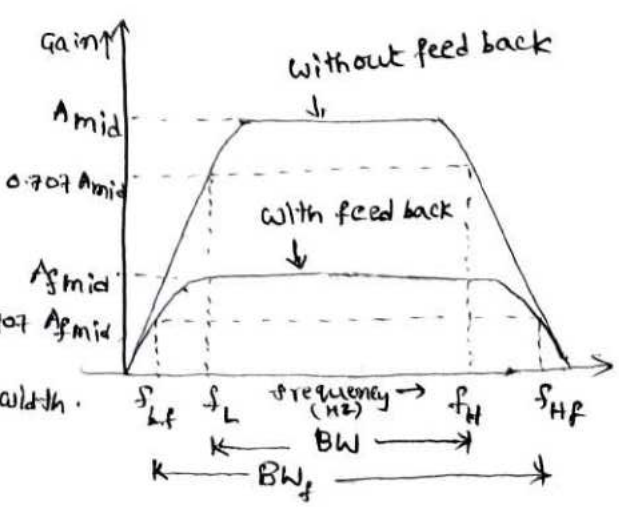
The bandwidth of an amplifier without feedback is given as $BW = f_H - f_L$.

The bandwidth of an amplifier with feedback is

$$BW_f = f_{Hf} - f_{Lf} = (1 + A_{mid}\beta)f_H - \frac{f_L}{(1 + A_{mid}\beta)}$$ or

it can also be written as $BW_f = BW(1 + A_{mid}\beta)$

It is very clear that $f_{Hf} - f_{Lf} > f_H - f_L$. So bandwidth of the amplifier with feedback is greater than the bandwidth of amplifier without feedback.



fig; Effect of negative - feedback on gain and bandwidth.

Note: As the voltage gain of the feedback amplifier reduces by a factor $1+A\beta$ and it's bandwidth increases by $1+A\beta$, the product of gain bandwidth product remains same for with feedback and for without feedback. $A_f \times BW_f = \left(\frac{A}{1+A\beta}\right) \times BW(1+A\beta)$

$$\therefore \boxed{A_f \times BW_f = A \times BW}$$

3) Frequency distortion: (or) Phase distortion reduction

If the feedback network doesnot contain reactive elements, the gain of the feedback amplifier is not a function of frequency. Under these circumstances the frequency distortion or Phase distortion can be reduced.

If feedback factor β is made up of reactive elements, the reactances of those elements will change with frequency, causing β to be changed. As a result feedback amplifier gain will also changes with frequency. So feedback network should be made up of passive elements.

4) Reduction in nonlinear distortion:

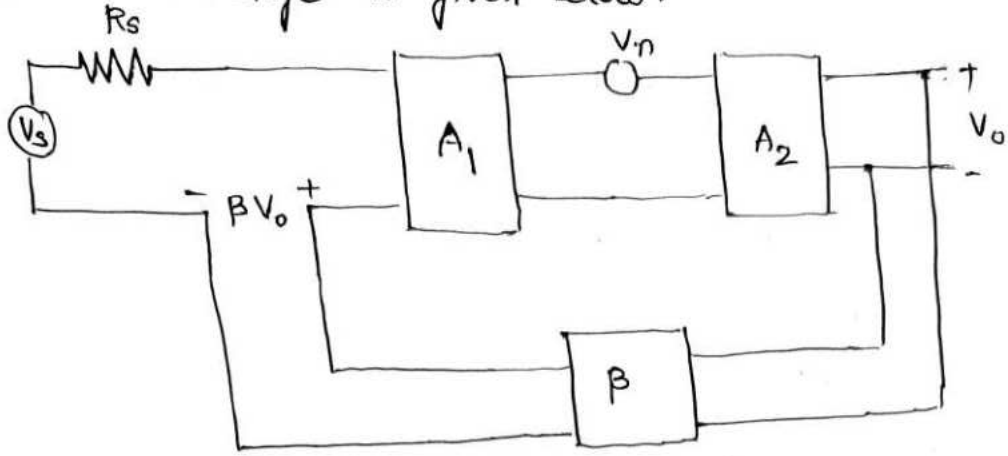
Consider a feed back amplifier with negative feed back, that has a basic amplifier with gain A and assume that the amplifier has the distortion 'D' without feedback and the distortion D_f with feed back. Then the distortion 'D' is reduced by a factor $1+A\beta$ and the distortion with feedback is given by $D_f = \frac{D}{1+A\beta}$.

5) Reduction in noise:

The negative feedback for an amplifier reduces the noise by increasing the ratio of signal to noise. Consider the amplifier block that has noise signal 'V_n' and gain A_2. Assume the input signal is V_s and the noise V_n is introduced at the second stage of amplifier as shown in below. The signal to noise ratio is given by

$$\frac{S}{N} = \frac{V_s}{V_n}.$$

The first stage of the amplifier with gain A_1 does not suffer from noise. This two stage amplifier with negative feedback having noise at 2nd stage is given below.



The output voltage V_o is given by

$$V_o = \frac{V_s A_1 A_2}{1+A_1A_2\beta} + \frac{V_n A_2}{1+A_1A_2\beta}$$

Signal to noise ratio at the output $= \left(\frac{V_s A_1 A_2}{1+A_1A_2\beta}\right) \Big/ \left(\frac{V_n A_2}{1+A_1A_2\beta}\right)$

$$\therefore \frac{S}{N} = \frac{V_s}{V_n} A_1$$

$\therefore$ Signal to noise ratio increases by a factor A_1. This improvement in signal to noise ratio results in reduction in noise.

The effect of negative feedback on input resistance:

Consider the negative feedback in an amplifier.

i) When the output of this negative feedback is connected to the input in series with the input signal the input resistance is increased. Since the feedback signal voltage V_f is out of phase with input voltage V_s that causes the input current I_i to be decreased and hence the input resistance with feedback $R_{if} = \frac{V_s}{I_i}$ is greater than the input resistance without feedback R_i. Hence the input resistance with feed back (R_{if}) for voltage series feedback and current series feedback is

$$R_{if} = R_i(1+A\beta) = R_i D.$$

ii) When the negative feedback signal is fed back to the input in shunt

with the amplifier input signal, then the input resistance is decreased. Since feedback current I_f and input current I_s are in out of phase then $I_i = I_s - I_f$. i.e $I_s = I_i + I_f$. Then the source input current I_s is increased and the input resistance with feed back $R_{if} = \frac{V_i}{I_s}$ is smaller than the input resistance without feedback i.e $R_{if} < R_i$. Hence for Voltage shunt and current shunt feedback amplifiers $R_{if} = \frac{R_i}{1+A\beta} = \frac{R_i}{D}$

That means the series mixing at input tends to increase the input resistance and the shunt mixing tends to decrease the input resistance.

1) Input resistance for Voltage series feed back amplifier: The following fig shows the voltage series feedback circuit with the input circuit and output circuit replaced by thevenin's model. In this circuit A_v represents the open circuit voltage gain taking R_s into account. We have considered R_s being the part of the amplifier for determing input resistance.

For the voltage series feedback amplifier input resistance with feedback $R_{if} = \frac{V_s}{I_i}$.

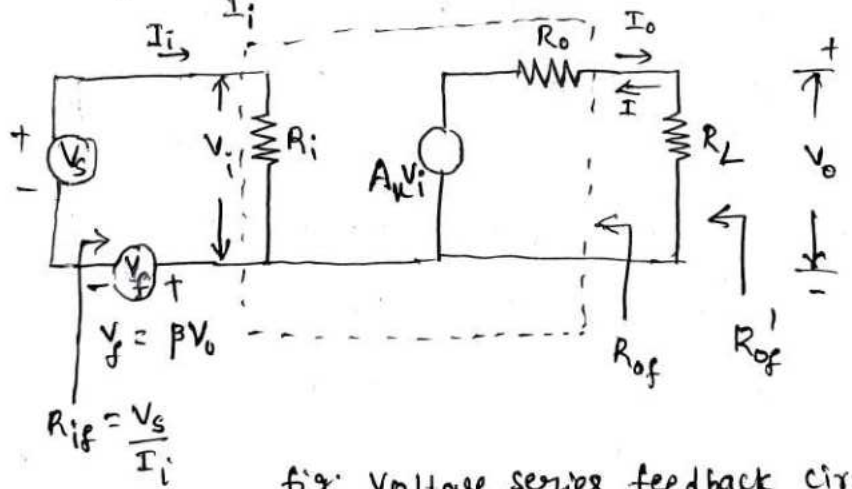


fig: Voltage series feedback circuit

Applying KVL to the input side $V_s = I_i R_i + V_f = I_i R_i + \beta V_o \rightarrow (1)$

out voltage $V_o = \frac{A_v V_i R_L}{R_o + R_L} = A_V V_i$ where $A_V = \frac{A_v R_L}{R_o + R_L} \rightarrow (2)$

From Equation ①, ② $V_s = I_i R_i + \beta V_o = I_i R_i + \beta A_V V_i$

$$\Rightarrow V_s = I_i R_i + \beta A_V I_i R_i$$

$$\Rightarrow V_s = I_i R_i (1 + \beta A_V)$$

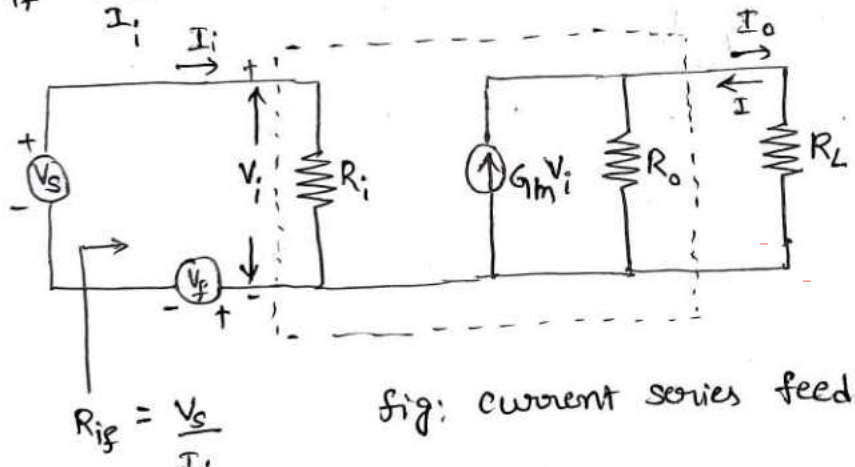
$$\therefore \frac{V_s}{I_i} = R_{if} = R_i (1 + \beta A_V)$$

where A_μ represents opencircuit voltage gain without feed back and A_V indicates the circuit voltage gain without feed back taking R_L into account. Therefore $A_\mu = \lim_{R_L \to \infty} A_V$

2) Input resistance for Current Series feedback amplifier:

Fig shows the current series feedback amplifier circuit with input circuit represented by thevenin's model and output circuit by Norton's equivalent circuit. Here input resistance with feedback is given by

$R_{if} = \frac{V_s}{I_i}$.



$V_f = \beta I_o$

$R_{if} = \frac{V_s}{I_i}$

fig: current series feedback amplifier circuit

Applying KVL to the input side,

$$V_s = I_i R_i + V_f = I_i R_i + \beta I_o \longrightarrow ①$$

The output current is written as

$$I_o = \frac{G_m V_i R_o}{R_o + R_L} = G_M V_i \longrightarrow ②$$

where $G_M = \frac{G_m R_o}{R_o + R_L}$

From equations ① and ② $V_s = I_i R_i + \beta I_o = I_i R_i + \beta G_M V_i$

$$\Rightarrow V_s = I_i R_i + \beta G_M I_i R_i$$

$$\Rightarrow V_s = I_i R_i (1+\beta G_M)$$

$$\Rightarrow \frac{V_s}{I_i} = R_i (1+\beta G_M)$$

$$\therefore \frac{V_s}{I_i} = R_{if} = R_i (1+\beta G_M)$$

where G_m represents short circuit transconductance without feedback and G_M represents transconductance without feed back taking R_L into account.

$$G_m = \lim_{R_L \to 0} G_M$$

3) Input resistance for current shunt feedback amplifier:

The fig' below shows the current shunt feedback amplifier circuit with input and output circuits replaced by norton's equivalent circuits. Here the input resistance with feedback is given by $R_{if} = \frac{V_i}{I_s}$.

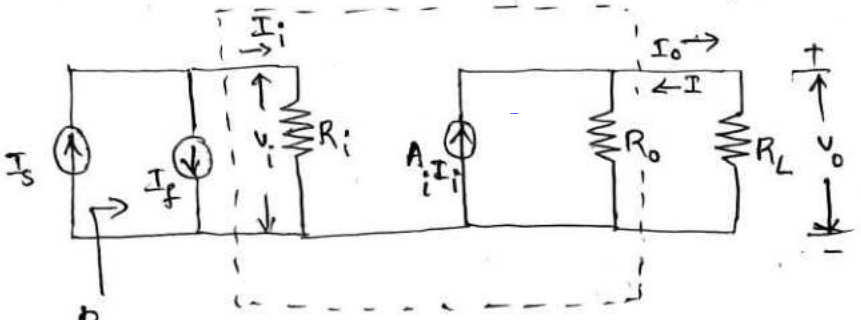


fig: Current shunt feedback amplifier circuit

Applying KCL at the input side $I_s = I_i + I_f = I_i + \beta I_o \longrightarrow (1)$

output current $I_o = \frac{A_i I_i R_o}{R_o + R_L} = A_I I_i \longrightarrow (2)$

where $A_I = \frac{A_i R_o}{R_o + R_L}$

From equations (1) and (2) $I_s = I_i + \beta A_I I_i = I_i (1+\beta A_I)$

$$\Rightarrow I_s = \frac{V_i}{R_i}(1+\beta A_I)$$

$$\therefore \frac{V_i}{I_s} = R_{if} = \frac{R_i}{1+\beta A_I}$$

where A_i represents the short circuit current gain without feedback and A_I represents the current gain without feedback taking R_L into account.

$$\therefore A_i = \lim_{R_L \to 0} A_I$$

4) Input resistance for Voltage Shunt feedback amplifier:

The following figure shows the voltage shunt feedback amplifier with input circuit is represented by Norton's equivalent circuit and the output circuit by thevenin's equivalent circuit. Here the input resistance with feedback is $R_{if} = \frac{V_i}{I_s}$

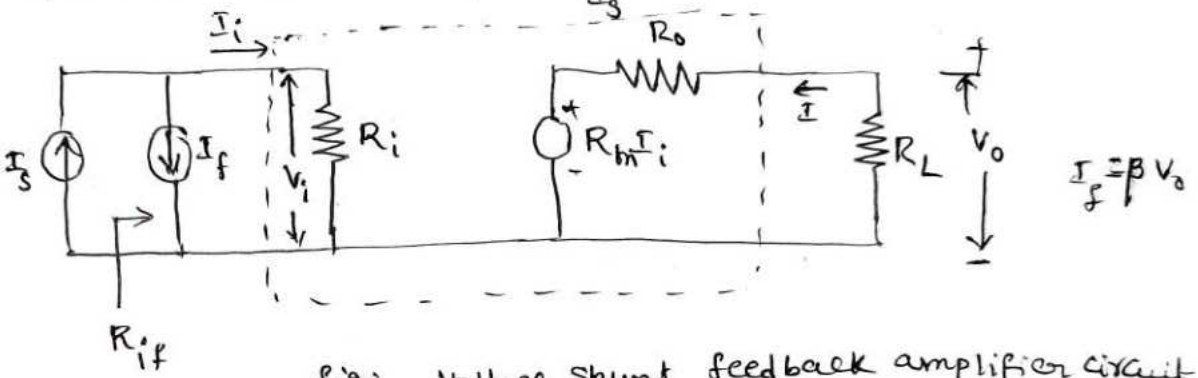


fig: Voltage shunt feedback amplifier circuit

Applying KCL at input circuit $I_s = I_i + I_f = I_i + \beta V_o \longrightarrow ①$

The output voltage $V_o = \frac{R_m I_i R_L}{R_o + R_L} = R_M I_i \longrightarrow ②$

where $R_M = \frac{R_m R_L}{R_o + R_L}$

From the equations ① and ② $I_s = I_i + \beta R_M I_i$

$$\Rightarrow I_s = I_i (1 + \beta R_M) = \frac{V_i}{R_i}(1 + \beta R_M)$$

$$\Rightarrow \frac{V_i}{I_s} = \frac{R_i}{1 + \beta R_M}$$

where R_m represents the open circuit transresistance without feedback and R_M represents the transresistance without feedback taking load R_L into account. Therefore $R_m = \lim_{R_L \to \infty} R_M$

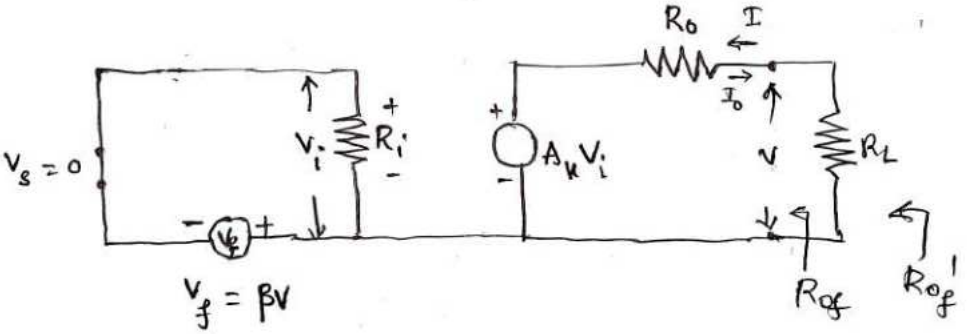
Effect of negative feedback on output resistance

The negative feedback which samples the output voltage irrespective of type of mixing at input side, decreases the output resistance. i.e voltage sampling causes the output resistance of the feedback amplifiers to decrease.

Similarly the negative feed back which samples the output current increases the output resistance irrespective of the type of mixing at input side. i.e current sampling increases the output resistance of the feedback amplifiers.

1) output resistance for a voltage series feedback amplifier:

In voltage series feedback amplifier the output resistance R_{of} is obtained by looking into the output terminals by disconnecting R_L (i.e $R_L = \infty$) and making source voltage V_s zero. (i.e $V_s = 0$)



Applying KVL to the output circuit

$$A_v V_i + I R_o = V \longrightarrow (1)$$

we know that $V_s - V_f = V_i$

Since $V_s = 0$, $V_i = -V_f$.

$$V_i = -(\beta V) \longrightarrow (2)$$

from equation (1) and (2)

$$A_v(-\beta V) + I R_o = V \qquad (\because V_f = \beta V \text{ with } V_s = 0)$$

$$V(1 + A_v\beta) = I R_o \Rightarrow \frac{V}{I} = \frac{R_o}{1 + A_v\beta}$$

$$\therefore \boxed{R_{of} = \frac{R_o}{1 + A_v\beta}}$$

Now $R_{of}' = R_{of} \| R_L$

$$= \left(\frac{R_o}{1+A_v\beta} \cdot R_L\right) \Big/ \left(\frac{R_o}{1+A_v\beta} + R_L\right)$$

$$\Rightarrow R_{of}' = \frac{R_o R_L}{R_o + R_L(1+A_v\beta)} = \frac{R_o R_L}{R_o + R_L + R_L A_v \beta}$$

Dividing numerator and denominator with $R_o + R_L$ we get

$$R_{of}' = \left(\frac{R_o R_L}{R_o + R_L}\right) \Big/ \left(1 + \frac{R_L A_v \beta}{R_o + R_L}\right)$$

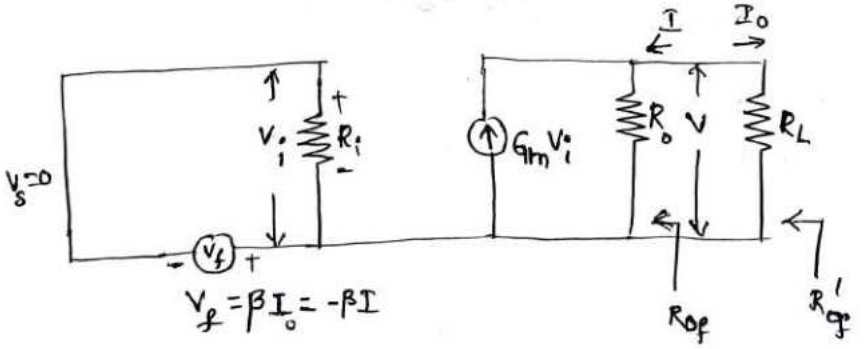
$$\boxed{R_{of}' = \frac{R_o'}{1 + A_V \beta}} \quad \left(\text{where } \frac{A_v R_L}{R_o + R_L} = A_V\right)$$

and $R_o' = \frac{R_o R_L}{R_o + R_L}$

where A_v is the open circuit voltage gain without feedback; and A_V is the voltage gain without feedback taking R_L into account.

2) output resistance for a current series feedback amplifier:

In this amplifier the output resistance is measured by looking into the output terminals disconnecting R_L (i.e $R_L = \infty$) and the external source voltage signal V_s is made zero.



Applying KCL to the output circuit $G_m V_i = \frac{V}{R_o} - I$

$$\Rightarrow I = \frac{V}{R_o} - G_m V_i \rightarrow (1)$$

we know that $V_s - V_f = V_i$

since $V_s = 0$, $-V_f = V_i$

$$\therefore V_i = -V_f = -(-\beta I) \rightarrow (2)$$

substituting equation (2) in equation (1) we get $I = \frac{V}{R_o} - G_m(\beta I)$

$$\Rightarrow I(1+G_m\beta) = \frac{V}{R_o}$$

$$\Rightarrow \frac{V}{I} = R_o(1+G_m\beta)$$

$$\therefore R_{of} = R_o(1+G_m\beta)$$

$$R_{of}' = R_{of} \| R_L = \frac{R_{of} R_L}{R_{of}+R_L} = \frac{R_o(1+\beta G_m) R_L}{R_o(1+\beta G_m)+R_L}$$

$$\Rightarrow R_{of}' = \frac{R_o R_L (1+\beta G_m)}{R_o + R_L + R_o \beta G_m}$$

Dividing numerator and denominator with $R_o + R_L$

$$R_{of}' = \frac{\left(\frac{R_o R_L}{R_o+R_L}\right)(1+\beta G_m)}{1+\frac{R_o \beta G_m}{R_o+R_L}} = \frac{R_o'(1+\beta G_m)}{1+\beta G_M}$$

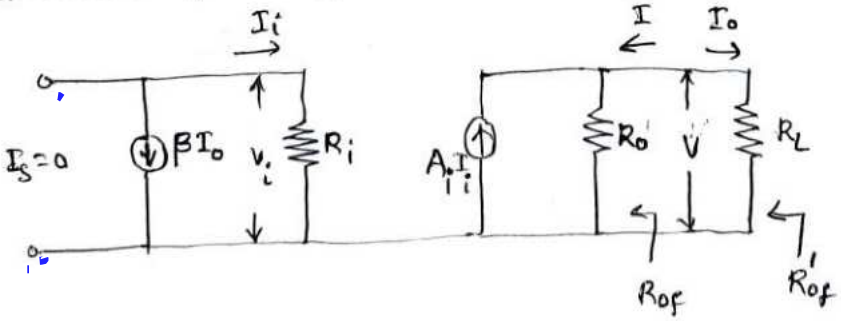
$$\therefore \boxed{R_{of}' = \frac{R_o'(1+\beta G_m)}{1+\beta G_M}} \quad \text{where } G_M = \frac{G_m R_o}{R_o+R_L}$$

Short circuit

where G_m is the transconductance without feedback and G_M is the transconductance without feedback taking R_L into account.

3) output resistance for a current shunt feedback amplifier:

In this amplifier the output resistance can be measured by looking into output terminals by disconnecting R_L and making the current source signal I_s zero.



Applying KCL at the output circuit we get

$$A_i I_i = \frac{V}{R_o} - I \quad \Rightarrow I = -A_i I_i + \frac{V}{R_o} \rightarrow (1)$$

we know that $I_s - I_f = I_i$

since $I_s = 0$, $I_i = -I_f = -\beta I_o = \beta I$ $(\because I_o = -I)$

$$\therefore I_i = \beta I \quad \rightarrow (2)$$

Substituting equation (2) in equation (1) we get

$$I = -A_i \beta I + \frac{V}{R_o}$$

$$\Rightarrow \quad I(1 + A_i\beta) = \frac{V}{R_o}$$

$$\Rightarrow \quad \frac{V}{I} = R_o(1 + A_i\beta)$$

$$\therefore R_{of} = R_o(1 + A_i\beta)$$

$$R'_{of} = R_{of} \| R_L = \frac{R_{of} R_L}{R_{of} + R_L} = \frac{R_o(1 + A_i\beta) R_L}{R_o(1 + A_i\beta) + R_L}$$

$$\Rightarrow R'_{of} = \frac{R_o R_L (1 + A_i\beta)}{R_o + R_L + R_o A_i \beta}$$

Divide the numerator and denominator by $R_o + R_L$

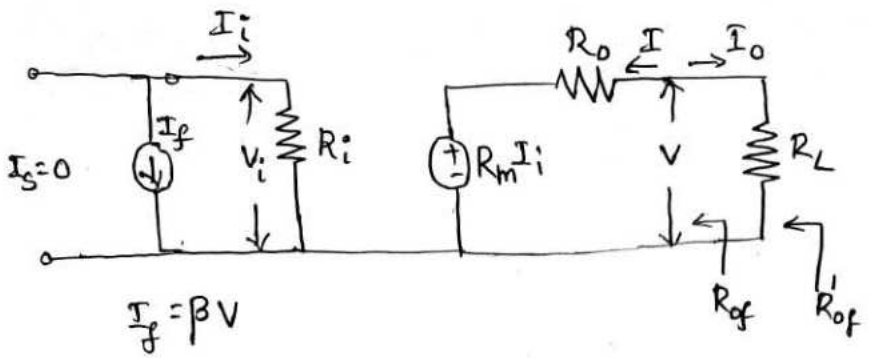
$$R'_{of} = \frac{\frac{R_o R_L}{R_o + R_L}(1 + A_i\beta)}{1 + \left(\frac{R_o}{R_o + R_L}\right) A_i \beta} = \frac{R'_o (1 + A_i\beta)}{1 + A_I \beta}$$

where $R'_o = R_o \| R_L$, $A_I = \frac{A_i R_o}{R_o + R_L}$

where A_i is the short circuit current gain without feedback and A_I is the current gain without feedback taking R_L into account

4) <u>output resistance of a voltage shunt feedback amplifier:</u>

In this amplifier the output resistance is measured by looking into output terminals by disconnecting R_L and making the current source signal I_s zero.



Applying KVL to the output side we get

$$V = R_m I_i + I R_o \longrightarrow (1)$$

We know that $I_s - I_f = I_i$.

Since $I_s = 0$ $\quad I_i = -I_f = -\beta V \longrightarrow (2)$

Substituting equation (2) in equation (1) we get

$$V = R_m(-\beta V) + I R_o$$

$$V(1 + \beta R_m) = + I R_o$$

$$\therefore \frac{V}{I} = \frac{R_o}{1+\beta R_m}$$

$$\therefore R_{of} = \frac{R_o}{1+\beta R_m}$$

$$R'_{of} = R_{of} \| R_L = \frac{R_{of} R_L}{R_{of} + R_L} = \frac{\frac{R_o}{1+\beta R_m} R_L}{\frac{R_o}{1+\beta R_m} + R_L}$$

$$\Rightarrow R'_{of} = \frac{R_o R_L}{R_o + R_L(1+\beta R_m)} = \frac{R_o R_L}{R_o + R_L + R_L \beta R_m}$$

Dividing the numerator and denominator by $R_o + R_L$

$$R'_{of} = \frac{\left(\frac{R_o R_L}{R_o + R_L}\right)}{1 + \frac{R_L R_m}{R_o + R_L} \cdot \beta} = \frac{R'_o}{1 + R_M \beta}$$

where $R'_o = \frac{R_o R_L}{R_o + R_L}$ and $R_M = \frac{R_L R_m}{R_o + R_L}$

R_m is open circuit transresistance without feedback, R_M is the transresistance without feedback, taking R_L into account.

Expression for transfer gain of a negative feedback amplifier:

Let the input signal from source as X_s, the output signal X_o, the feed back signal X_f and the input of the basic amplifier as X_i, each of these represents either voltage or Current.

Then the difference between the applied input signal X_s and the feed back signal X_f is called as the difference signal (or) error (or) comparison signal denoted by X_i (or) X_d, given as

$$X_d = X_s - X_f = X_i \rightarrow (1) \text{ for negative feed back.}$$

The reverse transmission factor (or) feedback ratio of the feedback network, β is given as $\beta = \frac{X_f}{X_o} \longrightarrow (2)$

The transfer gain (or) transfer ratio of basic amplifier is A, and is given as $A = \frac{X_o}{X_i} \longrightarrow (3)$

considering the negative feedback, the transfer gain of the amplifier with negative feedback (A_f) is given as

$$A_f = \frac{X_o}{X_s} \longrightarrow (4)$$

$$= \frac{X_o}{X_i + X_f} \quad (\because \text{from equation (1) } X_s = X_i + X_f)$$

$$= \frac{1}{\frac{X_i}{X_o} + \frac{X_f}{X_o}}$$

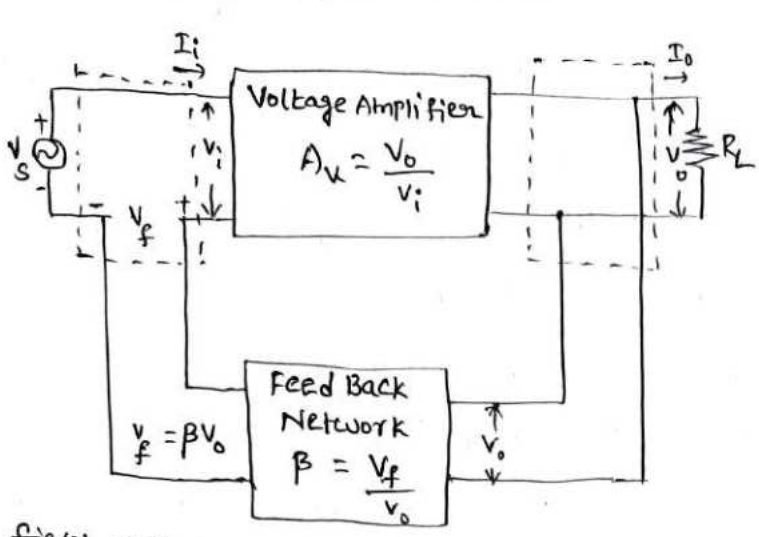
$$= \frac{1}{\frac{1}{A} + \beta} \quad (\because \text{from equations (2), (3)})$$

$$\therefore \boxed{A_f = \frac{A}{1 + A\beta}}$$

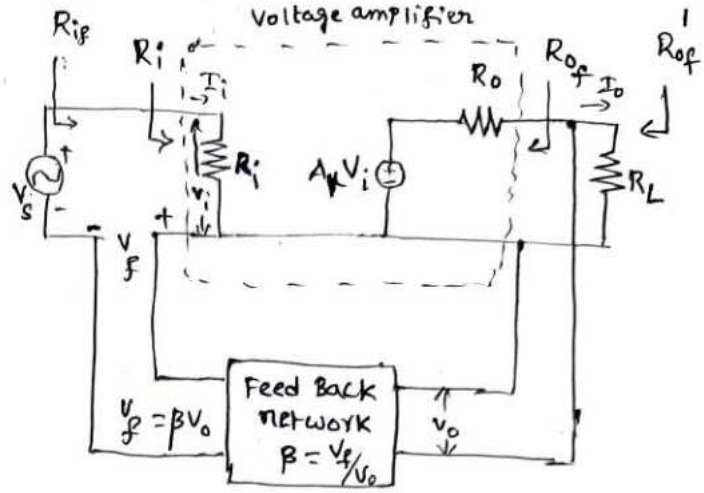
The expression for transfer gain of amplifier with negative feedback is denoted based on the type of basic amplifier.

The expression for transfergain of negative feedback amplifier for different basic amplifiers is derived below.

1) Transfer gain (or) Transfer ratio of a voltage series feed back amplifier:



fig(a) Voltage series feed back amplifier



fig(b): Equivalent circuit of Voltage series feedback amplifier.

* Figure (a) shows voltage series feedback amplifier, in which a part of the output voltage (V_f) is fed back in series with the input signal (V_s).

* The sampler used in voltage series feedback amplifier is voltage sampler. For voltage sampling the output voltage V_o is connected in shunt with the input of feed back network that has a feedback ratio of β.

* For combining the output of feedback network (V_f) with the input voltage (V_s), a series mixer is used i.e the output voltage of feedback network (V_f) is fed back in series with the input signal (V_s).

* The difference between V_s and V_f is applied as an input to the voltage amplifier, when the feed back connection is negative feedback.

$$\text{i.e} \quad V_i = V_s - V_f \longrightarrow (1)$$

Feedback ratio of the feedback network is β and is given as

$$\beta = \frac{V_f}{V_o} \longrightarrow (2)$$

The transfer gain of the voltage amplifier is A_v and is given as

$$A_v = \frac{V_o}{V_i} \longrightarrow (3)$$

The transfer gain of the voltage amplifier with feedback is given as

$$A_{vf} = \frac{V_o}{V_s} = \frac{V_o}{V_i + V_f} \quad (\because \text{from equation (1)}\ V_s = V_i + V_f)$$

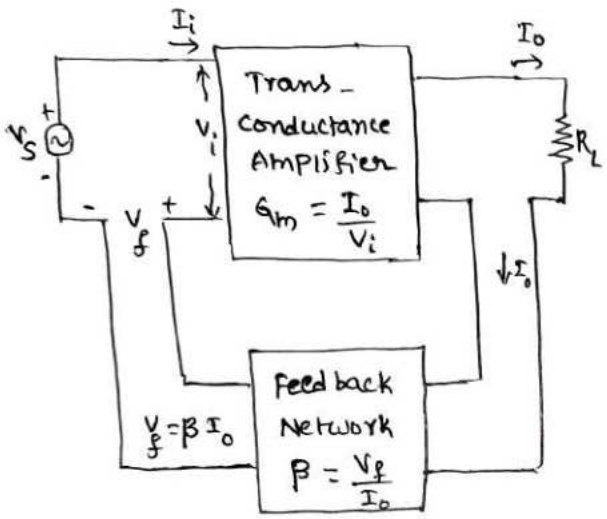
$$\Rightarrow A_{Vf} = \frac{1}{\frac{V_i}{V_o} + \frac{V_f}{V_o}}$$

$$\Rightarrow A_{Vf} = \frac{1}{\frac{1}{A_V} + \beta} \qquad (\because \text{from equations } ②, ③)$$

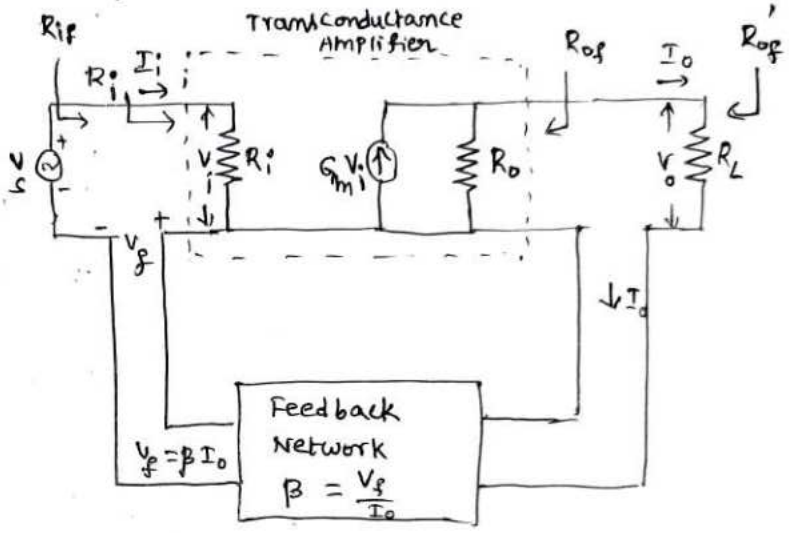
$$\therefore \boxed{A_{Vf} = \frac{A_V}{1 + A_V \beta}}$$

This equation says that the voltage gain with feedback is equal to the voltage amplifier gain reduced by a factor $1 + A_V\beta$.

2) Transfer gain (or) Transfer ratio of a current series feedback amplifier:



fig(a): Current series feedback Amplifier



fig(b): Equivalent Circuit of Current series feed back amplifier

* Figure (a) shows the current series feedback amplifier in which the value of the output current I_o is proportional to the developed voltage V_i.

* Here current sampler is used in a current series feedback amplifier. For current sampling the output current I_o is connected in series with the input of feedback network.

* For combining the output of feedback network (V_f) and the input voltage (V_s), a series mixer is used. i.e the output voltage (V_f) of the feedback network is fed back in series with the input voltage (V_s).

* The difference between V_s and V_f is applied as the input to

the transconductance amplifier, when feedback connection is negative feedback ie $V_i = V_s - V_f \longrightarrow (1)$

Feedback ratio of the feedback network is $\beta = \frac{V_f}{I_o} \rightarrow (2)$

The transfer gain of the transconductance amplifier is G_m and is given as $G_m = \frac{I_o}{V_i} \longrightarrow (3)$

The transfer gain of the trans Conductance amplifier with feedback is G_{mf} and is given as $G_{mf} = \frac{I_o}{V_s} = \frac{I_o}{V_i + V_f}$ ($\because$ from eq (1) $V_s = V_i + V_f$)

$$\Rightarrow G_{mf} = \frac{1}{\frac{V_i}{I_o} + \frac{V_f}{I_o}}$$

$$\Rightarrow G_{mf} = \frac{1}{\frac{1}{\frac{I_o}{V_i}} + \frac{V_f}{I_o}}$$

$$\Rightarrow G_{mf} = \frac{1}{\frac{1}{G_m} + \beta}$$ ($\because$ From equations (2), (3))

$$\therefore \boxed{G_{mf} = \frac{G_m}{1 + G_m \beta}}$$

This equation says that the transconductance with feedback is equal to transconductance without feedback reduced by a factor $1 + G_m \beta$

3) Transfer gain (or) transfer ratio of a Current Shunt feedback amplifier

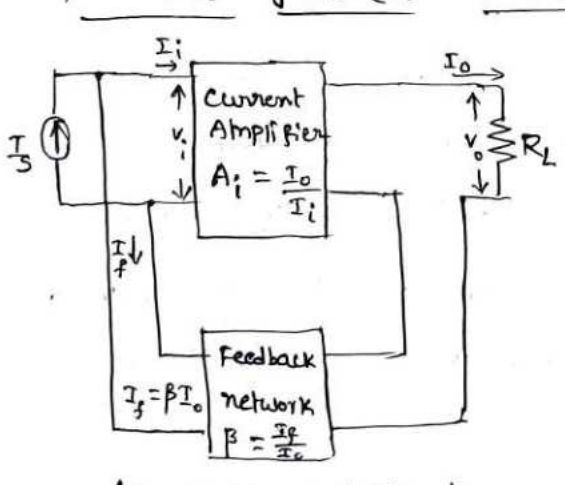


fig (a) : Current shunt - feed back amplifier

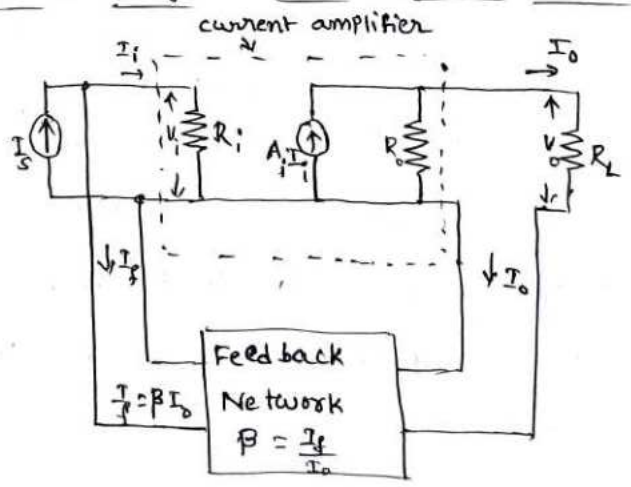


fig (b) : Equivalent circuit of a Current - Shunt feedback amplifier.

* figure(a) shows the current shunt feedback amplifier block diagram
* In this amplifier, the current sampler is used. For current sampling the output current I_o is connected in series with the input of the feedback network.
* For combining the output of feedback network (I_f) and the input current I_s, a shunt mixer is used. i.e the output current I_f of the feedback network is fedback in shunt with the input current I_s.
* The difference between I_s and I_f is applied as the input to the current amplifier provided the feedback connection is negative feedback.

$$\text{i.e } I_i = I_s - I_f \longrightarrow (1)$$

Feed Back ratio of the feedback network is β given as

$$\beta = \frac{I_f}{I_o} \longrightarrow (2)$$

The transfer gain of current amplifier is A_i and is given as

$$A_i = \frac{I_o}{I_i} \longrightarrow (3)$$

The transfergain of current amplifier with negative feedback is given as

$$A_{if} = \frac{I_o}{I_s} = \frac{I_o}{I_i + I_f} \quad \left(\because \text{from equation (1)}\ I_s = I_i + I_f\right)$$

$$= \frac{1}{\left(\frac{I_i}{I_o}\right) + \left(\frac{I_f}{I_o}\right)}$$

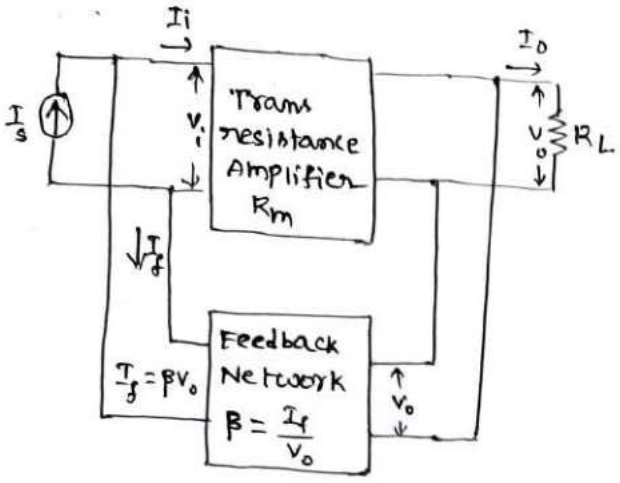
$$= \frac{1}{\frac{1}{\left(\frac{I_o}{I_i}\right)} + \frac{I_f}{I_o}}$$

$$= \frac{1}{\frac{1}{A_i} + \beta} \quad (\because \text{from equations (2), (3)})$$

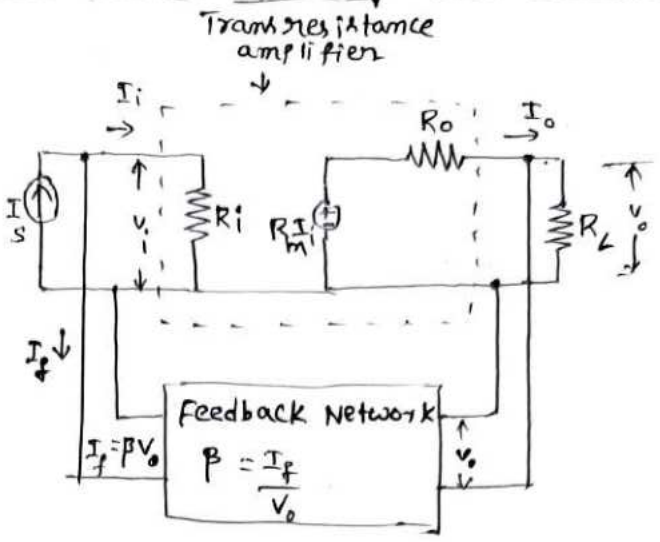
$$\therefore \boxed{A_{if} = \frac{A_i}{1 + A_i\beta}}$$

the above equation says that the current gain with negative feedback is equal to the Current gain without feedback reduced by a factor of $1 + A_i\beta$.

4) Transfer gain (or) transfer ratio of a voltage shunt feedback amplifier:



fig(a): Voltage shunt feedback Amplifier



fig(b): Equivalent circuit of a voltage - shunt feedback amplifier.

* figure (a) shows the voltage shunt feedback amplifier block diagram.
* In this amplifier the voltage sampler is used. For voltage sampling the output voltage (V_o) is connected in parallel with the input of the feedback network.
* For combining the output current (I_f) of the feedback network and the input current I_s, shunt mixing is used. i.e the output current (I_f) of the feedback network is fedback in parallel to the Input current (I_s).
* The difference between I_s and I_f is applied as the input to the transresistance amplifier provided the feedback is negative feedback.

$$\text{ie} \quad I_i = I_s - I_f \longrightarrow (1)$$

Feedback ratio of the feedback network is β and is given as

$$\beta = \frac{I_f}{V_o} \longrightarrow (2)$$

The transfer gain of the transresistance amplifier is R_m given as

$$R_m = \frac{V_o}{I_i} \longrightarrow (3)$$

The transfer gain of the transresistance amplifier with feedback is R_{mf} given as $R_{mf} = \frac{V_o}{I_s} = \frac{V_o}{I_i + I_f}$ ($\because$ from equation ① $I_s = I_i + I_f$)

$$\Rightarrow R_{mf} = \frac{1}{\frac{I_i}{V_o} + \frac{I_f}{V_o}}$$

$$= \frac{1}{\frac{1}{R_m} + \beta} \quad (\because \text{from equations ②, ③})$$

$$\therefore \boxed{R_{mf} = \frac{R_m}{1 + R_m\beta}}$$

The above equation says, the transresistance with negative feedback is equal to the transresistance without feedback reduced by a factor of $1 + R_m\beta$.

Method of analysis of a feedback amplifier:

For analysing the feedback amplifier it is necessary to go through the following steps.

Step1: Identify the topology (type of feedback)

(a) To identify the type of sampling:

i) By shorting the output node (ie making $V_o = 0$), if the feedback signal becomes zero, then it is called voltage sampling

ii) By opening the output loop (i.e making $I_o = 0$), if the feedback signal becomes zero, then it is called current sampling

(b) To identify the type of mixing:

i) If the feedback signal is subtracted from the externally applied signal as a voltage in the input loop it is called series mixing.

ii) If the feedback signal is subtracted from the externally applied signal as a current in the input loop, it is called shunt mixing.

Step2: To find the input circuit

i) For voltage sampling, the output voltage is made zero by shorting the output node.

ii) for current sampling, the output current is made zero by opening the output loop.

Step3: To find the output circuit

i) For series mixing, the input current is made zero by opening the input loop.

ii) For shunt mixing, the input voltage is made zero by shorting the input node.

From step2 and step3 ensure that the feedback is reduced to zero, without altering the loading on the basic amplifier.

Step4: Replace each active device by proper model. for example the hybrid-π model for a transistor at high frequencies, or the h-parameter model at low frequencies.

Step5: Find A, i.e the open loop gain of the amplifier (gain without feedback).

Step6: Indicate X_f (i.e whether V_f (or) I_f) and X_o (i.e whether V_o (or) I_o) on the circuit and evaluate $\beta = X_f/X_o$.

Step7: From A and β find D, A_f, R_{if}, R_{of} and R_{of}'.

Comparison among the characteristics of feedback amplifiers:

Topology / Characteristics	Voltage series	Current series	Current shunt	Voltage shunt
1) Feed back signal (X_f)	Voltage (V_f)	Voltage (V_f)	Current (I_f)	Current (I_f)
2) Sampled signal (X_o)	Voltage (V_o)	Current (I_o)	Current (I_o)	Voltage (V_o)
3) To find the input circuit	Set $V_o = 0$	Set $I_o = 0$	Set $I_o = 0$	Set $V_o = 0$
4) To find the output circuit	Set $I_i = 0$	Set $I_i = 0$	Set $V_i = 0$	Set $V_i = 0$
5) Signal source	Thevenin	Thevenin	Norton	Norton
6) $\beta = \frac{X_f}{X_o}$	V_f/V_o	V_f/I_o	I_f/I_o	I_f/V_o
7) $A = \frac{X_o}{X_i}$	$A_V = V_o/V_i$	$G_M = I_o/V_i$	$A_I = \frac{I_o}{I_i}$	$R_M = \frac{V_o}{I_i}$
8) Desensitivity $D = 1+A\beta$	$1 + A_V\beta$	$1 + G_M\beta$	$1 + A_I\beta$	$1 + R_M\beta$
9) $A_f = A/(1+A\beta)$	$A_{Vf} = A_V/(1+A_V\beta)$	$G_{Mf} = G_M/(1+G_M\beta)$	$A_{If} = A_I/(1+A_I\beta)$	$R_{Mf} = R_M/(1+R_M\beta)$
10) R_{if}	$R_i(1+A_V\beta)$	$R_i(1+G_M\beta)$	$R_i/(1+A_I\beta)$	$R_i/(1+R_M\beta)$
11) R_{of}	$R_o/(1+A_V\beta)$	$R_o(1+G_M\beta)$	$R_o(1+A_i\beta)$	$R_o/(1+R_M\beta)$
12) R_{of}'	$R_o'/(1+A_V\beta)$	$R_o'(1+G_M\beta)/(1+G_M\beta)$	$R_o'(1+A_i\beta)/(1+A_I\beta)$	$R_o'/(1+R_M\beta)$

Problems

1) The distortion in amplifier is found to be 3%, when the feedback ratio of negative feedback amplifier is 0.04. when the feedback is removed, the distortion becomes 15%. Find the open loop gain & closed loop gain

Sol) Given negative feed back amplifier having feedback ratio $\beta = 0.04$

Distortion in amplifier with negative feedback is $D_f = 3\%$.

i.e $D_f = 0.03$

Distortion in amplifier when feed back is removed $D = 15\% = 0.15$

we know that $D_f = \frac{D}{1+A\beta} \Rightarrow 0.03 = \frac{0.15}{1+A(0.04)}$

$\Rightarrow 0.03 + A(0.0012) = 0.15$

$\therefore$ open loop gain $(A) = 100$

closed loop gain $A_f = \frac{A}{1+A\beta}$ for negative feed back

$= \frac{100}{1+(100)(0.04)}$

$\therefore A_f = 20$

$\therefore$ open loop gain $A = 100$, closed loop gain $A_f = 20$.

2) An amplifier has midband voltage gain 500 with lower and upper cutoff frequencies as 100Hz and 100KHz respectively. If 5% feedback is applied find lower and upper cut off frequencies with feed back.

sol) Given $A_{Vmid} = 500$, $f_L = 100Hz$, $f_H = 100KHz$

feedback factor $\beta = 5\% = 0.05$

$f_{Lf} = ?$ $f_{Hf} = ?$

we know that f_{Lf} for negative feed back is given as

$f_{Lf} = \frac{f_L}{1+A_{mid}\beta} = \frac{100}{1+(500)(0.05)} = 3.84615\ Hz$

f_{Hf} for negative feed back amplifier is

$f_{Hf} = f_H(1+A_{mid}\beta) = 100\times10^3\left(1+(500)(0.05)\right)$

$\therefore f_{Hf} = 2.6MHz$

$\therefore$ lower cutoff frequency with feedback $f_{Lf} = 3.84615\ Hz$

upper cutoff frequency with feed back $f_{Hf} = 2.6\ MHz$.

3) A voltage series negative feedback amplifier has a voltage gain without feedback of $A = 50$, input resistance $R_i = 2K\Omega$, output resistance $R_o = 15K\Omega$, feed back ratio of 0.01. Calculate the voltage gain, input resistance and output resistance of amplifier with feedback.

Sol) Given A negative feed back voltage series amplifier.

Voltage gain without feed back $A_V = 50$

Input resistance without feedback $R_i = 2K\Omega$

output resistance without feed back $R_o = 15K\Omega$

Feedback ratio $\beta = 0.01$

Voltage gain with feedback $A_{Vf} = \frac{A_V}{1 + A_V\beta} = \frac{50}{1+(50)(0.01)} = 33.3333$

Input resistance with feed back $R_{if} = R_i(1 + A_V\beta)$

$= 2\times10^3(1 + 50(0.01))$

$\therefore R_{if} = 3K\Omega$

output resistance with feedback $R_{of} = \frac{R_o}{1+A_V\beta} = \frac{15\times10^3}{1+(50(0.01))}$

$\therefore R_{of} = 10K\Omega$

4) An amplifier has a midband gain of 1500 and a bandwidth of 4MHZ. The midband gain reduces to 150 when a negative feedback is applied. Determine the value of feedback factor and the bandwidth.

Sol) Given $A_{mid} = 1500$, $BW = 4MHZ = 4\times10^6$ HZ

Mid band Gain reduces to 150 when negative feed back is applied.

i.e $A_{fmid} = 150$, Let feed back factor $= \beta$

we know that $A_{fmid} = \frac{A_{mid}}{1 + A_{mid}\beta}$

$\Rightarrow \quad 150 = \frac{1500}{1+(1500\beta)}$ 10

$\Rightarrow \quad 1 + 1500\beta = 10 \Rightarrow 1500\beta = 9$

$\therefore$ feedback factor $\beta = 0.006$

Bandwidth with negative feedback $BW_f = BW(1 + A_{mid}\beta)$

$= 4\times10^6(1 + (1500\times0.006))$

$\therefore$ Bandwidth with negative feedback $(BW_f) = 40MHZ$

5) An amplifier with 2.5kΩ input resistance and 50kΩ output resistance has a voltage gain of 100. the amplifier is now modified to provide 5% negative feed back in series with the input. Calculate the voltage gain, input resistance & output resistance with feedback.

Sol) Given $A_V = 100$, $R_i = 2.5k\Omega$, $R_o = 50k\Omega$

Given Feedback factor $\beta = 0.05$ ($\because 5\%$) negative feedback.

Voltage gain with feed back $A_{Vf} = \frac{A_V}{1+A_V\beta} = \frac{100}{1+(100)(0.05)} = 16.6666$

According to the given data the amplifier here we have is voltage-series feed back amplifier, for which $R_{if} = R_i(1+A_V\beta)$ and

$$R_{of} = \frac{R_o}{1+A_V\beta}$$

Input resistance with feed back $R_{if} = R_i(1+A_V\beta)$

$= 2.50\times10^3 (1+(100)(0.05))$

$\therefore R_{if} = 15\ k\Omega$

output resistance with feed back $R_{of} = \frac{R_o}{1+A_V\beta} = \frac{50\times10^3}{1+(100)(0.05)}$

$\therefore R_{of} = 8.333\ k\Omega$

6) An amplifier has an open loop gain of 1000 and feedback ratio of 0.04. If the open loop gain changes by 10% due to temperature, find the percentage change in gain of the amplifier with feedback

Sol) Given open loop gain $A = 1000$

feed back ratio $\beta = 0.04$

Refer Problem No(13) (wrong method)

Gain of amplifier with feed back $A_f = \frac{A}{1+A\beta} = \frac{1000}{1+(1000)(0.04)}$

$\Rightarrow A_f = 24.39024$

The open loop gain changes by 10% due to temperature variation.

$\therefore$ New open loop gain $A_1 = 1000 + 10\%$ of $1000 = 1100$.

Gain of amplifier with feed back $A_{1f} = \frac{A_1}{1+A_1\beta} = \frac{1100}{1+(100)(0.04)} = 24.444444$

% change in gain of the amplifier with feed back $= \frac{24.44444 - 24.39024}{24.39024} \times 100$

$\therefore$ % change in gain of amplifier with feedback $= 0.2222\%$

(7) The voltage gain of an amplifier without feedback is 60dB. It decreases to 40dB with feed back. Calculate feed back factor.

Sol) Given voltage gain of an amplifier with out feedback = 60 dB

$$\text{i.e } 20 \log_{10} A_V = 60$$

$$\log_{10} (A_V) = 3$$

$$A_V = 1000.$$

Voltage gain with feedback = 40 dB

$$\text{i.e } 20 \log_{10} A_{Vf} = 40$$

$$\log_{10} A_{Vf} = 2$$

$$A_{Vf} = 100.$$

Feedback factor $\beta = ?$

we know that $A_{Vf} = \frac{A_V}{1 + A_V \beta} \Rightarrow 100 = \frac{1000}{1 + (1000\beta)}$

$$\Rightarrow 1 + 1000\beta = 10$$

$$\therefore \text{feedback factor } (\beta) = 0.009$$

8) An amplifier with negative feedback has a gain of 50. It is found that without feedback, an input signal of 0.1V is required to produce a given output. Where as with feedback the input signal must be 0.8V for the same output. Calculate the voltage gain and feedback ratio.

Sol) Given $A_{Vf} = 50$,

$V_i = 0.1V$,

$V_o = ?$

with feedback the i/p signal must be equal to 0.8V.

$$\text{i.e } V_s = V_i + V_f = 0.8V$$

$$\Rightarrow V_s = 0.1 + V_f = 0.8V$$

$$V_f = 0.7V.$$

we know that $A_{Vf} = \frac{V_o}{V_s} = 50$

$$\Rightarrow \frac{V_o}{0.8} = 50 \Rightarrow V_o = 40V.$$

Voltage gain without feed back $A_V = \frac{V_o}{V_i} = \frac{40}{0.1} = 400$

Feedback factor $(\beta) = \frac{V_f}{V_o} = \frac{0.7}{40} = 0.0175$

9) A current shunt feedback amplifier has a current gain of 100, $Z_i = 2K\Omega$, $Z_o = 15K\Omega$, find A_{if}, Z_{if}, Z_{of}. $\beta = 0.05$

Sol) Given $A_i = 100$, $\beta = 0.05$, $Z_i = 2K\Omega$, $Z_o = 15K\Omega$

$$A_{if} = \frac{A_i}{1+A_i\beta} = \frac{100}{1+(100)(0.05)} = 16.6666$$

$$Z_{if} = \frac{Z_i}{1+A_i\beta} = \frac{2\times10^3}{1+(100)(0.05)} = 333.333\Omega$$

$$Z_{of} = Z_o(1+A_i\beta) = 15\times10^3(1+(100)(0.05)) = 90K\Omega$$

10) A current series feedback amplifier has $G_M = 500\mho$, $R_i = 3K\Omega$ $R_o = 30K\Omega$, $\beta = 0.01$. Find G_{Mf}, R_{if}, R_{of}.

Sol) Given $G_M = 500\mho$ $R_i = 3K\Omega$ and $R_o = 30K\Omega$. $\beta = 0.01$

$$G_{Mf} = \frac{G_M}{1+G_M\beta} = \frac{500}{1+((500)(0.01))} = 83.3333\mho$$

$$R_{if} = R_i(1+G_M\beta) = 3\times10^3(1+(500)(0.01)) = 18\ K\Omega$$

$$R_{of} = R_o(1+G_M\beta) = 30\times10^3(1+(500)(0.01)) = 180K\Omega$$

11) A voltage shunt feedback amplifier has $R_M = 300\Omega$, $R_i = 2K\Omega$ and $R_o = 20K\Omega$. $\beta = 0.05$. Find R_{Mf}, R_{if} and R_{of}

Sol) Given $R_M = 300\Omega$, $R_i = 2K\Omega$, $R_o = 20K\Omega$

$$R_{Mf} = \frac{R_M}{1+R_M\beta} = \frac{300}{1+(300)(0.05)} = 18.75\Omega$$

$$R_{if} = \frac{R_i}{1+R_M\beta} = \frac{2\times10^3}{1+(300)(0.05)} = 125\Omega$$

$$R_{of} = \frac{R_o}{1+R_M\beta} = \frac{20\times10^3}{1+(300)(0.05)} = 1.25K\Omega.$$

12) An amplifier has a midband gain of 125 and a bandwidth of 250KHZ. a) If 4 j. -ve feedback is applied find new bandwidth and new gain b) If Bandwidth is restricted to 1MHZ find β value

Sol) Given $A_{mid} = 125$, $BW = 250\,KHZ$,

a) $\beta = 4\% = 0.04$ with negative feedback.

New Bandwidth $BW_f = BW(1 + A_{mid}\beta) = 250\times10^3(1+(125\times0.04))$

$BW_f = 1.5\,MHZ$

New Gain with negative feedback $A_f = \frac{A}{1+A\beta} = \frac{125}{1+(125)(0.04)} = 20.8333$

b) BW_f' is given as $BW_f' = 1MHZ$, then $\beta' = ?$

$BW_f' = BW(1 + A_{mid}\beta')$

$1\times10^6 = 250\times10^3(1 + 125\beta)$

$\Rightarrow \beta' = 0.024 = 2.4\%$

13) An amplifier has an open loop gain of 1000, feedback ratio of 0.04. If the open loop gain changes by 10% due to temperature. Find the percentage change in the gain of amplifier with feedback.

Sol) Given open loop gain $(A) = 1000$,

feedback ratio $(\beta) = 0.04$.

Given the fractional change in open loop gain $= \frac{dA}{A} = 10\% = 0.1$

Fractional change (percentage change) in gain of the amplifier, with feedback $= \frac{dA_f}{A_f} = ?$

we know that the sensitivity $S = \frac{\left(\frac{dA_f}{A_f}\right)}{\left(\frac{dA}{A}\right)} = \frac{1}{1+A\beta}$

$\Rightarrow \frac{\left(\frac{dA_f}{A_f}\right)}{0.1} = \frac{1}{1+(1000)(0.04)}$

$\Rightarrow \frac{dA_f}{A_f} = \frac{0.1}{41} = 0.002439$

$\Rightarrow \frac{dA_f}{A_f} = 0.2439\%$

$\therefore$ Percentage change in the gain of the amplifier with feed back i.e $\frac{dA_f}{A_f} = 0.2439\%$

14) An amplifier has a voltage gain with feedback of 100. If the gain without feedback changes by 20% and the gain with feedback is restricted to 2%, determine the open loop gain and feedback factor.

Sol) Given the voltage gain with feedback $A_f = 100$.

Fractional change in the gain without feed back $= \frac{dA}{A} = 20\% = 0.2$

Fractional change in the gain with feed back $= \frac{dA_f}{A_f} = 2\% = 0.02$

we know that $\left(\frac{dA_f}{A_f}\right) \Big/ \left(\frac{dA}{A}\right) = \frac{1}{1+A\beta}$

$\Rightarrow \quad \frac{0.02}{0.2} = \frac{1}{1+A\beta}$

$\Rightarrow \quad 1 + A\beta = 10$

we know that $A_f = \frac{A}{1+A\beta} \qquad (\because A_f = 100)$

$\Rightarrow \quad 100 = \frac{A}{10} \qquad (\because 1+A\beta = 10)$

$\Rightarrow \quad A = 1000$

$1 + A\beta = 10 \quad \Rightarrow \quad 1 + (1000\beta) = 10$

$\therefore \beta = 0.009$

$\therefore$ Open loop gain(A) = 1000, feed back factor $\beta = 0.009$.

15) An amplifier has open loop gain of 4000 and a feedback ratio of 0.05. If the open loop gain changes by 15% due to temperature Find the percentage change in the gain of the amplifier with feed back.

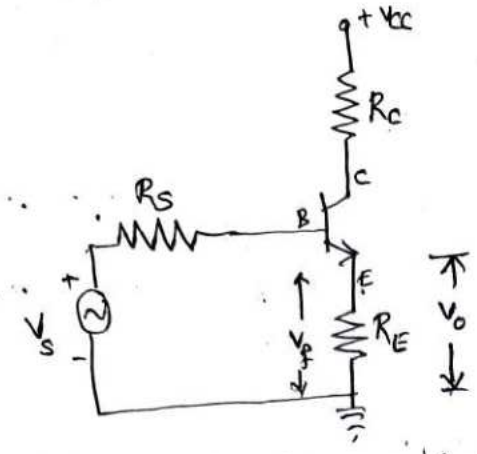
Sol) Given $A = 4000$, $\beta = 0.05$

$\frac{dA}{A} = 15\% = 0.15, \quad \frac{dA_f}{A_f} = ?$

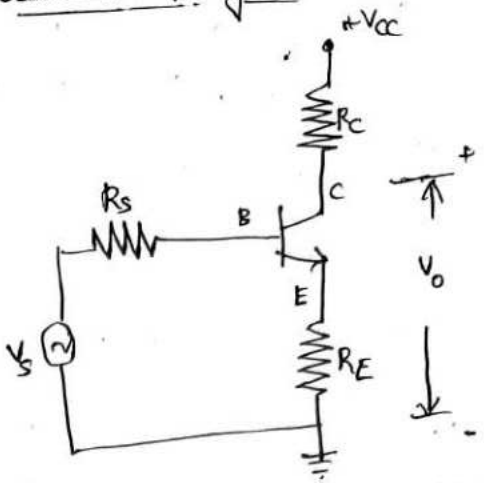
we know that $\frac{dA_f}{A_f} = \frac{(dA/A)}{1+A\beta} = \frac{0.15}{1+(4000)(0.05)}$

$\therefore \frac{dA_f}{A_f} = 0.07462\%$

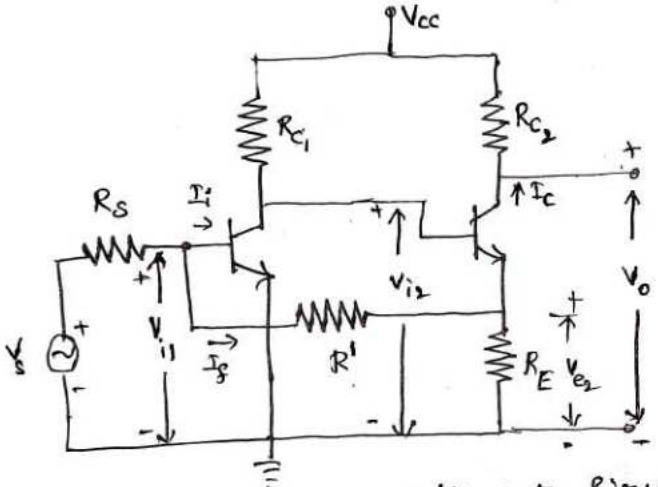
Practical circuits for different feedback topologies:



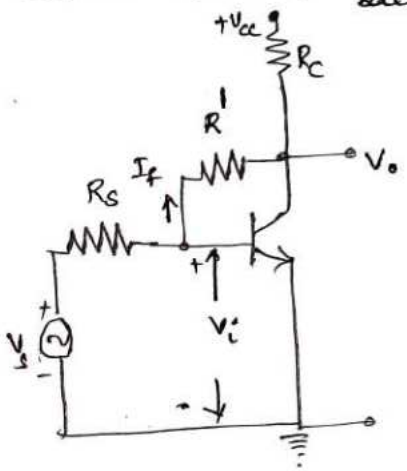
fig(a) BJT Emitter follower circuit (for voltage series feedback Amplifier)



fig(b): CE amplifier with unbypassed Emitter resistor (current series feedback amplifier)



fig(c): Second transistor emitter to first transistor base feedback pair (for Current Shunt feedback amplifier)



fig(d): Common Emitter with a resistor R' connected between input and output (for voltage Shunt feedback amplifier)

Explain the characteristics of negative feedback (or) Explain the effects of negative feedback on amplifier characteristics:

1) Stabilization of Gain:

The gain of the amplifier with negative feedback is

$$A_f = \frac{A}{1+A\beta} \rightarrow (1)$$

Differentiating the A_f with respect to A

$$\frac{dA_f}{dA} = \frac{(1+A\beta)(1) - A(\beta)}{(1+A\beta)^2} = \frac{1}{(1+A\beta)^2}$$

$$\Rightarrow \quad dA_f = \frac{dA}{(1+A\beta)^2}$$

2) Extension of bandwidth:

The difference between the upper cut off frequency and lower cut off frequency is called as the bandwidth of an amplifier given as Bandwidth $(BW) = f_H - f_L$.

The bandwidth of the amplifier with feedback increases by a factor of $(1+A\beta)$ i.e $BW_f = BW(1+A\beta)$. Because, due to negative feedback upper cut off frequency f_{Hf} is increased by a factor $(1+A\beta)$ and lower cut off frequency f_{Lf} is decreased by the same factor $(1+A\beta)$. i.e $f_{Hf} = f_H(1+A\beta)$, $f_{Lf} = \frac{f_L}{1+A\beta}$.

3) Frequency Distortion reduction (or) Phase distortion reduction:

If the feedback network does not contain reactive elements, the gain of the feedback amplifier is not a function of frequency. Under these circumstances the frequency distortion (or) phase-distortion can be reduced.

If feedback factor β is made up of reactive elements, the reactances of those elements will change with frequency, causing β to be changed. As a result feedback amplifier gain will also changes with frequency. so feedback network should be made up of passive elements.

4) Reduction in nonlinear distortion and noise:

The negative feedback introduced to an amplifier reduces both noise and nonlinear distortion by a factor $(1+A\beta)$. Thus noise and nonlinear distortion also reduced by the same factor as that of transfer gain.

5) Increase in input resistance:

An amplifier should have high input resistance. If the feedback signal is combined with the input source signal in series (i.e if the mixer used is a series mixer) the input resistance R_i increases with a factor $1+A\beta$. i.e $R_{if} = R_i(1+A\beta)$.

$$\Rightarrow \frac{dA_f}{A_f} = \frac{dA}{A_f(1+A\beta)^2}$$

$$\Rightarrow \frac{dA_f}{A_f} = \frac{dA}{\frac{A}{1+A\beta}(1+A\beta)^2}$$

$$\Rightarrow \left(\frac{dA_f}{A_f}\right) \Big/ \left(\frac{dA}{A}\right) = \frac{1}{1+A\beta}$$

$\therefore$ Sensitivity $S = \left(\frac{dA_f}{A_f}\right) \Big/ \left(\frac{dA}{A}\right) = \frac{1}{1+A\beta}$

Desensitivity $D = \frac{1}{S} = 1+A\beta$

The stability of the amplifier increases if the desensitivity is increased.

The gain of the amplifier is not constant as it depends on the factors such as temperature, aging of components, and temperature dependent parameters. This lack of stability can be reduced by introducing negative feedback.

The gain of amplifier with negative feedback is

$$A_f = \frac{A}{1+A\beta}$$

If $A\beta >> 1$ then $A_f = \frac{1}{\beta}$ and gain is dependent only on feedback network. Hence maintaining $A\beta >> 1$ and constructing feedback network only with stable passive elements a good stability is achieved.

Then for voltage series feedback $A_{Vf} = \frac{1}{\beta}$, voltage gain is stabilized

for Current series feedback $G_{Mf} = \frac{1}{\beta}$, transconductance is stabilized

For current shunt feedback $A_{If} = \frac{1}{\beta}$, Current gain is stabilized.

For voltage shunt feedback $R_{Mf} = \frac{1}{\beta}$, transresistance is stabilized

Thus the input resistance is increased with series mixer using negative feedback irrespective of the type of sampling.

6) Decrease in output resistance:

An amplifier with low output resistance is capable of delivering maximum power to the load without much loss. For such a low output resistance negative feedback is very helpful. The output resistance can be decreased by using a voltage sampler irrespective of the type of mixer; by a factor $(1+A\beta)$.

$$\text{i.e} \quad R_{of} = \frac{R_o}{1+A\beta} .$$

Effect of negative feedback on amplifier characteristics:

Characteristics	Type of feedback			
	Voltage series	Current series	Current shunt	Voltage shunt
Transfer gain	Decreases	Decreases	Decreases	Decreases
Bandwidth	Increases	Increases	Increases	Increases
Nonlinear Distortion	Decreases	Decreases	Decreases	Decreases
Noise	Decreases	Decreases	Decreases	Decreases
Input resistance	Increases	Increases	Decreases	Decreases
output resistance	Decreases	Increases	Increases	Decreases

UNIT - II
SINUSOIDAL OSCILLATORS

INTRODUCTION:

↦ Any circuit which is used to generate a periodic voltage without an ac input signal is called an oscillator. To generate the AC voltage the circuit is supplied with energy from a dc source.

↦ If the output voltage is a sine wave function of time, the oscillator is called as a sinusoidal oscillator (or) Harmonic oscillator.

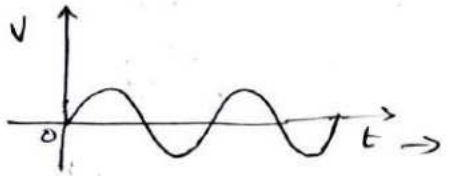
↦ There is an other category of oscillators which generate non-sinusoidal wave forms such as square, sawtooth, triangular or rectangular etc.

Classification of oscillators:

The oscillators can be classified in different ways.

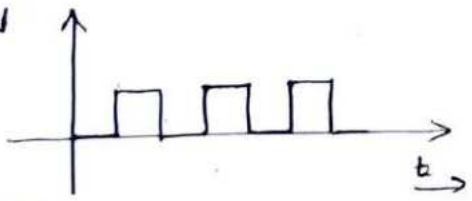
1) According to the wave forms generated
   a) sinusoidal oscillators
   b) Relaxation oscillators.

- sinusoidal oscillator generates voltage or current which is a sinewave function of time as shown in figure(a)

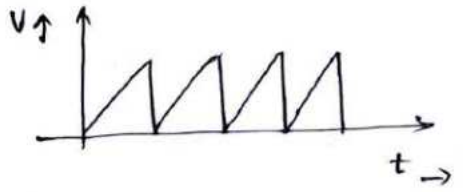


fig(a): sinusoidal wave form

- A relaxation oscillator generates voltage or current which vary abruptly one or more times in a cycle of oscillation as shown in figure(b) and fig(c).



fig(b) square wave form



fig(c): sawtooth wave form.

2) According to the fundamental mechanisms involved
   a) Negative resistance oscillators
   b) Feedback oscillators

- In a negative resistance oscillator the negative resistance of the amplifying device is used to neutralize the positive resistance of the oscillator.

- Feedback oscillator is formed by using the positive feedback in a feedback amplifier such that it satisfies the Barkhausen criterion.

3) According to the frequency generated

a) Audio Frequency oscillator : 20Hz to 20KHz
b) Radio Frequency oscillator : 20KHz to 30MHz
c) Very High Frequency oscillator : 30MHz to 300MHz
d) Ultra high Frequency oscillator : 300MHz to 3GHz
e) Microwave Frequency oscillator : 3GHz and above.

4) According to the type of the circuit used, Sinusoidal oscillators are classified as

a) LC Tuned oscillator
b) RC Phase shift oscillator.

Concept of Positive feedback :

If some portion of the output signal is fed back to the input of the amplifier in phase with the external signal from source, such feedback is known as positive feedback.

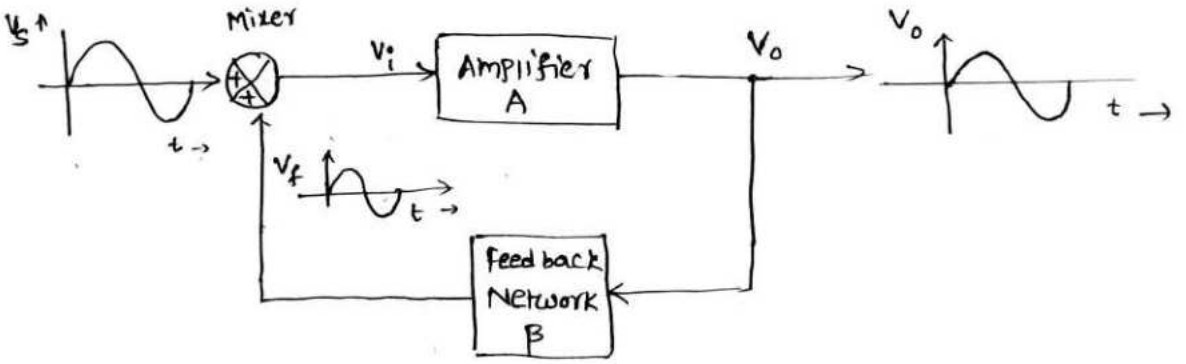


fig: Concept of positive feedback

Assume that a sinusoidal input signal V_s is applied to the circuit. The output of the amplifier as V_o. Some portion of the output signal is taken from the output of feedback network as V_f which is in phase with V_s. Hence V_f is added with V_s to give the input to the amplifier as V_i i.e $V_i = V_s + V_f$ ⟶ (1)

Let the gain of the amplifier without feed back as A

Then $A = \frac{V_o}{V_i}$ ⟶ (2)

The feedback factor of the feedback network 'β' is given as

$$\beta = \frac{V_f}{V_0} \longrightarrow (3)$$

The gain of the amplifier with feedback is A_f given as

$$A_f = \frac{V_0}{V_s} \longrightarrow (4)$$

$$= \frac{V_0}{V_i - V_f} \quad \left(\because \text{from eq } (1),\ V_s = V_i - V_f \right)$$

$$= \frac{1}{\left(\frac{V_i}{V_0}\right) - \left(\frac{V_f}{V_0}\right)}$$

$$= \frac{1}{\frac{1}{A} - \beta} \quad (\because \text{equation } (2) \text{ and } (3))$$

$$\therefore \boxed{A_f = \frac{A}{1 - A\beta}}$$

Conditions for oscillation (or) Barkhausen Criterion:

The oscillator circuit produces oscillations due to the random variation in the base current due to the noise component (or) a small variation in the DC supply. The noise components of extremely small electrical voltages are always present in the circuit environment, that causes small signal at the output of the amplifier, even in the absence of the external signal. Let the amplifier is tuned to a particular frequency f_0, hence the output signal produced due to noise will also be of frequency f_0. If a small fraction (β) of the output signal is fed back to the input, then this feedback signal will be amplified by the amplifier.

If the amplifier has a gain of more than $\frac{1}{\beta}$, then the output goes on increasing, but as the output increases, the gain of the amplifier decreases and at a particular value of output, the gain of the amplifier is reduced exactly equal to $\frac{1}{\beta}$. Then the output remains constant at frequency f_0. This frequency f_0 is called as frequency of oscillation.

The essential conditions for maintaining oscillations are

1) $|A\beta| = 1$ i.e the magnitude of loop gain must be unity.

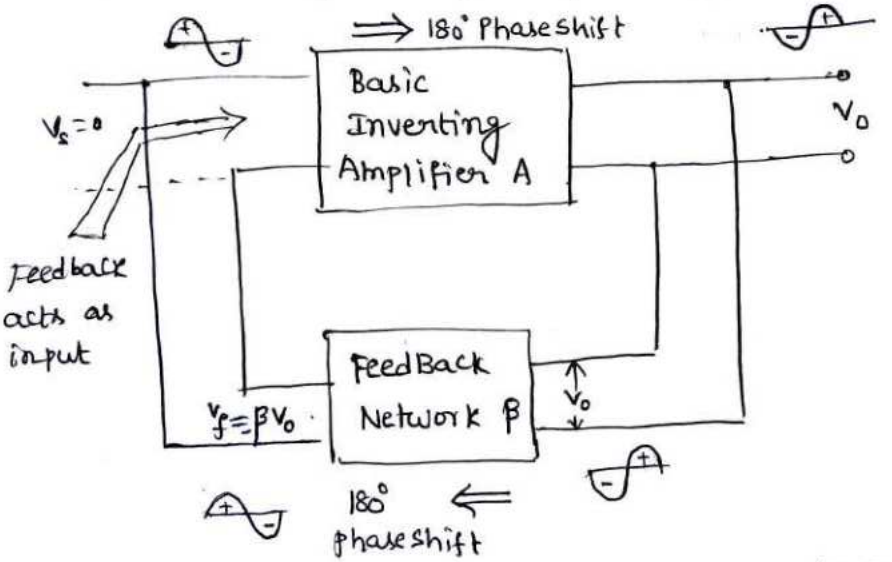
2) The total Phase shift around the closed loop is zero or 360°.

Consider an inverting basic amplifier with open loop gain A, which produces 180° Phase shift between it's input and output. And the feedback network has a feedback factor β. Assume $V_s = 0$.

An output is generated at the amplifier due to the variations in dc (or) due to noise from which a fraction of the output is fed back to the input of the amplifier through feedback network. This feed back signal acts as input V_i to the circuit now.

open loop gain $A = \frac{V_o}{V_i} \rightarrow (1)$

Feedback signal $V_f = -\beta V_o \rightarrow (2)$ '-' sign indicates 180° Phase shift



Since V_f is going as V_i here $V_f = V_i$

eq (1) $\Rightarrow V_o = AV_i = A \cdot V_f$

$\therefore V_o = A \cdot V_f \rightarrow (3)$

Substituting equation (3) in equation (2) we get

$$V_f = -\beta A V_f$$

$$\Rightarrow A\beta = -1$$

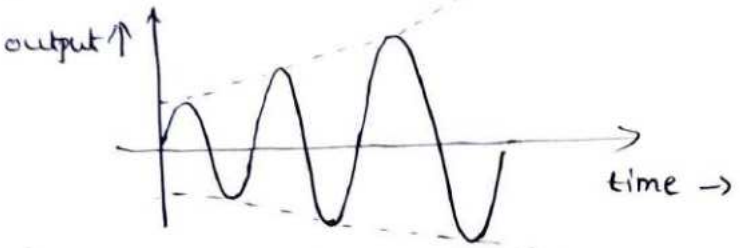
$$\Rightarrow A\beta = -1 + j0$$

$$\therefore |A\beta| = 1$$

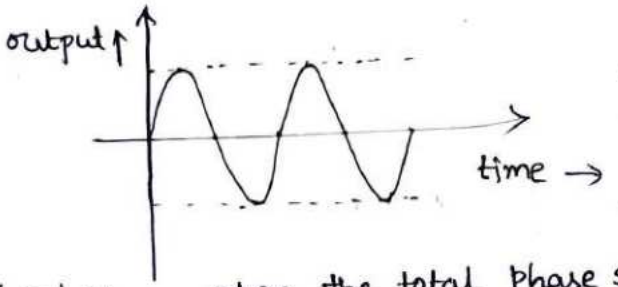
Here the basic inverting amplifier introduces 180° phase shift, in addition to which 180° phase shift should be provided by the feedback network to make the total phase shift around the closed loop as 360°.

Effect of magnitude of loop gain $|A\beta|$ on nature of oscillations:

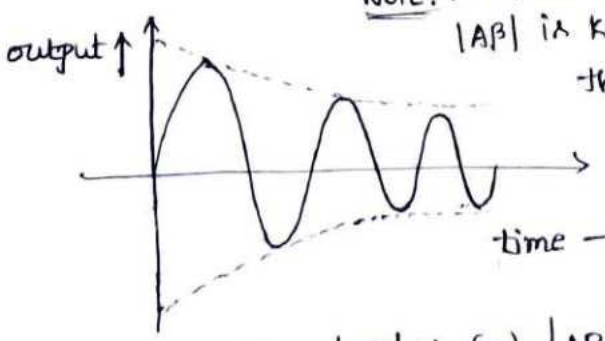
i) when $|A\beta| > 1$: when the total phase shift around the closed loop is 0° or 360° and $|A\beta| > 1$ then the output contains the oscillations of growing type. i.e the amplitude of oscillations goes on increasing.



ii) when $|A\beta| = 1$: when the total phase shift around the closed loop is 0° or 360° and $|A\beta| = 1$ then the output contains the oscillations with constant frequency and amplitude, these oscillations are called as sustained oscillations. (or) undamped oscillations.



iii) when $|A\beta| < 1$: when the total phase shift around the closed loop is 0° or 360° and $|A\beta| < 1$ then the oscillations are of decaying type i.e the amplitude decreases exponentially.



NOTE: To start oscillations without input $|A\beta|$ is kept higher than unity and then the circuit adjust itself to get $|A\beta| = 1$ to result sustained oscillations.

NOTE: The oscillations under $|A\beta| < 1$ (or) $|A\beta| > 1$ are called as under damped (or) over damped oscillations resp.

LC oscillators :

General form of an LC oscillator :

The general form of an LC oscillator requires any one of the active devices such as Transistor, FET, Vacuum tube, and op-amp may be used in the amplifier section.

Z_1, Z_2, and Z_3 are the reactive elements constituting the feedback tank circuit which determines the frequency of oscillation. Here Z_1 and Z_2 serve as an ac voltage divider for the output voltage and the feedback signal.

The voltage across Z_1 is the feedback signal.

The frequency of oscillation of an LC oscillator is

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

The general form of an LC oscillator and it's equivalent circuit are as shown in below, in which the output terminals are 2 and 3, and input terminals are 1 and 3.

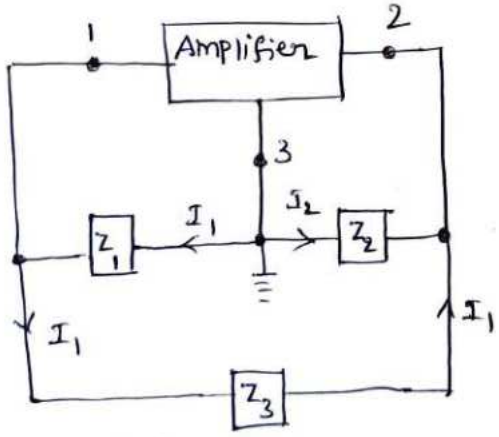


fig (a) General form of an LC oscillator

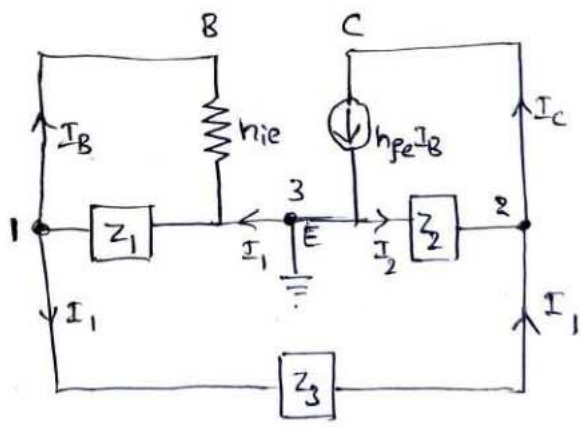


fig (b) : Equivalent Circuit of an LC oscillator.

Load impedance : (Z_L)

Since Z_1 is in parallel with the resistance hie, their equivalent resistance Z' is given by

$$\frac{1}{Z'} = \frac{1}{Z_1} + \frac{1}{h_{ie}}$$

$$\therefore Z' = \frac{Z_1 h_{ie}}{Z_1 + h_{ie}} \longrightarrow (1)$$

Now the load impedance Z_L is the impedance between the terminals 2 and 3 (i.e output terminals) which is equal to Z_2 in parallel with $Z' + Z_3$.

$$\text{i.e } \frac{1}{Z_L} = \frac{1}{Z_2} + \frac{1}{Z' + Z_3}$$

$$\Rightarrow \frac{1}{Z_L} = \frac{1}{Z_2} + \frac{1}{\frac{Z_1 h_{ie}}{Z_1 + h_{ie}} + Z_3}$$

$$= \frac{1}{Z_2} + \frac{Z_1 + h_{ie}}{Z_1 h_{ie} + Z_1 Z_3 + Z_3 h_{ie}}$$

$$= \frac{1}{Z_2} + \frac{Z_1 + h_{ie}}{(Z_1 + Z_3) h_{ie} + Z_1 Z_3}$$

$$= \frac{h_{ie}(Z_1 + Z_3) + Z_1 Z_3 + Z_2 h_{ie} + Z_1 Z_2}{Z_2 \left[h_{ie}(Z_1 + Z_3) + Z_1 Z_3 \right]}$$

$$= \frac{h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2 + Z_1 Z_3}{Z_2 \left[h_{ie}(Z_1 + Z_3) + Z_1 Z_3 \right]}$$

$$\therefore Z_L = \frac{Z_2 \left[h_{ie}(Z_1 + Z_3) + Z_1 Z_3 \right]}{h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2 + Z_1 Z_3} \longrightarrow (2)$$

Voltage Gain without feed back (A_V)

$$\text{Voltage Gain } (A_V) = \frac{A_I Z_L}{Z_i} = -\frac{h_{fe} Z_L}{h_{ie}} \longrightarrow (3)$$

Feedback factor (β) :

The output voltage between the terminals 3 and 2 in terms of current I_1 is given by $V_0 = -I_1 (Z' + Z_3) = -I_1 \left(\frac{Z_1 h_{ie}}{Z_1 + h_{ie}} + Z_3 \right)$

$$V_0 = -I_1 \left(\frac{h_{ie}(Z_1 + Z_3) + Z_1 Z_3}{Z_1 + h_{ie}} \right) \longrightarrow (4)$$

the voltage fed back to the terminals 3 and 1 is given by

$$V_f = -I_1 Z' = -I_1 \left(\frac{Z_1 h_{ie}}{Z_1 + h_{ie}} \right) \longrightarrow (5)$$

The feed back ratio $\beta = \frac{V_f}{V_0} = -I_1 \left(\frac{Z_1 h_{ie}}{Z_1 + h_{ie}} \right)$ ($\because$ from eq (4), (5))

$$-I_1 \left(\frac{h_{ie}(Z_1 + Z_3) + Z_1 Z_3}{Z_1 + h_{ie}} \right)$$

$$\Rightarrow \quad \beta = \frac{Z_1 h_{ie}}{h_{ie}(Z_1 + Z_3) + Z_1 Z_3} \longrightarrow (6)$$

The equation for the oscillator

For producing oscillations $A_V \beta = 1$ is the condition

substituting eq (3) and eq (6) in this equation we get

$$\frac{-h_{fe} Z_L}{h_{ie}} \left[\frac{Z_1 h_{ie}}{h_{ie}(Z_1 + Z_3) + Z_1 Z_3} \right] = 1$$

$$\Rightarrow \quad \frac{h_{fe} Z_L Z_1}{h_{ie}(Z_1 + Z_3) + Z_1 Z_3)} = -1 \text{ , substituting } Z_L \text{ from equation (2)}$$

$$\Rightarrow \quad \frac{h_{fe} Z_1}{h_{ie}(Z_1 + Z_3) + Z_1 Z_3} \left[\frac{Z_2 \left[h_{ie}(Z_1 + Z_3) + Z_1 Z_3 \right]}{h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2 + Z_1 Z_3} \right] = -1$$

$$\Rightarrow \quad \frac{h_{fe} Z_1 Z_2}{h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2 + Z_1 Z_3} = -1$$

$$\Rightarrow \quad h_{fe} Z_1 Z_2 = -\left[h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2 + Z_1 Z_3 \right]$$

$$h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2 (1 + h_{fe}) + Z_1 Z_3 = 0 .$$

This is the general equation for the oscillator.

Hartley oscillator:

In the Hartley oscillator Z_1 and Z_2 are inductors and Z_3 is a capacitor. The Hartley oscillator circuit is as shown in below.

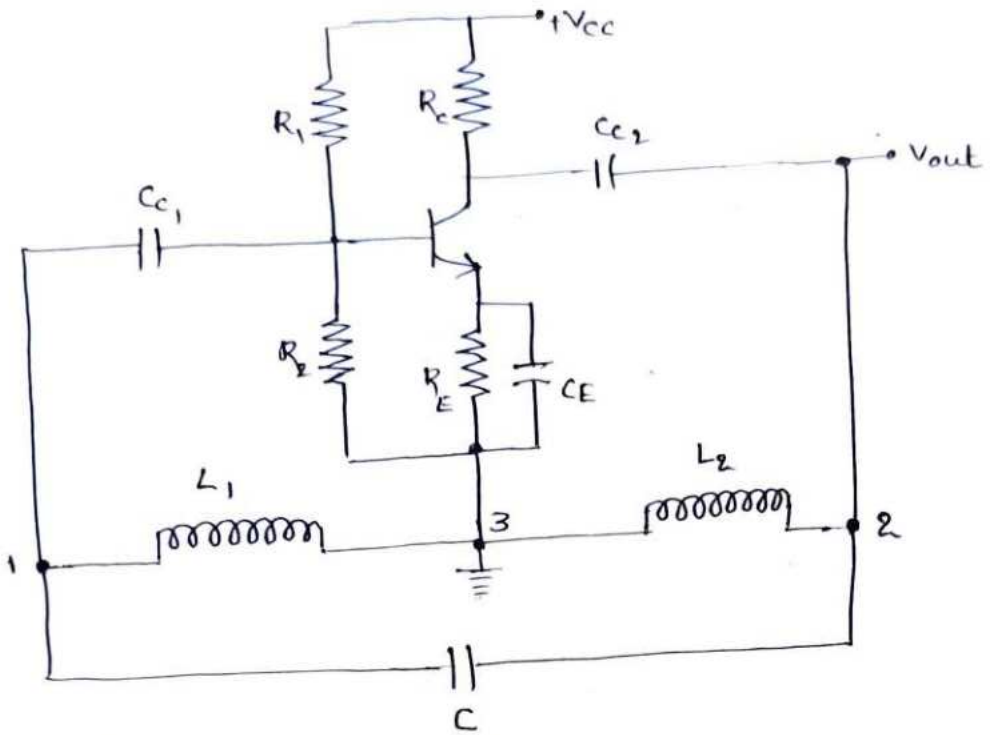


fig: Hartley oscillator

Here the resistors R_1, R_2 and R_E provides the required bias to the transistor. C_E is a bypass capacitor, C_{c_1} and C_{c_2} are the coupling capacitors. The feedback network consists of the inductors L_1 and L_2 and capacitor C determines the frequency of oscillation.

When the supply voltage $+V_{cc}$ is turned ON, a transient current is produced in the tank circuit. The current in the tank circuit develops AC voltages across L_1 and L_2. As the terminal 3 is grounded, it is at zero potential. If terminal 1 is at a positive potential with respect to terminal 3 at any instant, the terminal 2 will be at negative potential with respect to terminal 3 at the same instant. Thus the phase difference between the terminals 1 and 2 is always 180°. In the CE mode, the transistor produces 180° phase difference between input and output. Therefore the total phase shift is 360°. Thus at the frequency determined for the tank circuit, the necessary condition for sustained oscillations is satisfied.

If the feedback is adjusted such that the loop gain $A\beta = 1$, the circuit acts as an oscillator.

The frequency of oscillation is $f_o = \frac{1}{2\pi\sqrt{LC}}$

where $L = L_1 + L_2 + 2M$ and M is the mutual inductance value between L_1 and L_2 coils.

The condition for sustained oscillation is

$$h_{fe} \geq \frac{L_1 + M}{L_2 + M}.$$

Analysis: In the Hartley oscillator, Z_1 and Z_2 are inductive reactances and Z_3 is the capacitive reactance. Suppose 'M' is the mutual inductance between the inductors, then

$$Z_1 = j\omega L_1 + j\omega M$$

$$Z_2 = j\omega L_2 + j\omega M$$

$$Z_3 = \frac{1}{j\omega C} = \frac{-j}{\omega C}$$

we know the general equation for the oscillator is

$$h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2 (1 + h_{fe}) + Z_1 Z_3 = 0$$

Substituting Z_1, Z_2 and Z_3 in this equation from above equations,

$$h_{ie}\left(j\omega L_1 + j\omega M + j\omega L_2 + j\omega M - \frac{j}{\omega C}\right) + (j\omega L_1 + j\omega M)(j\omega L_2 + j\omega M)(1 + h_{fe}) + (j\omega L_1 + j\omega M)\left(\frac{-j}{\omega C}\right) = 0$$

$$j\omega h_{ie}\left(L_1 + L_2 + 2M - \frac{1}{\omega^2 C}\right) - \omega^2 (L_1 + M)(L_2 + M)(1 + h_{fe}) + (L_1 + M)\frac{1}{C} = 0$$

$$j\omega h_{ie}\left(L_1 + L_2 + 2M - \frac{1}{\omega^2 C}\right) - \omega^2 (L_1 + M)\left[(L_2 + M)(1 + h_{fe}) - \frac{1}{\omega^2 C}\right] = 0 \quad \hookrightarrow (1)$$

The frequency of oscillation $f_o = \frac{\omega_o}{2\pi}$ is determined by equating the imaginary part of the above equation to zero by substituting $\omega = \omega_o$ i.e $\omega_o h_{ie}\left(L_1 + L_2 + 2M - \frac{1}{\omega_o^2 C}\right) = 0$

$$\Rightarrow \quad \frac{1}{\omega_0^2 C} = L_1 + L_2 + 2M$$

$$\Rightarrow \quad \omega_0^2 = \frac{1}{(L_1+L_2+2M)C}$$

$$\therefore \quad \omega_0 = \frac{1}{\sqrt{(L_1+L_2+2M)C}} \longrightarrow (2)$$

$$f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{(L_1+L_2+2M)C}} \longrightarrow (3)$$

The condition for maintenance of oscillation is obtained by substituting eq (3) in eq (1) which makes the imaginary part to zero. Hence

$$(L_2+M)(1+h_{fe}) - \frac{1}{\omega_0^2 C} = 0$$

$$\Rightarrow \quad (L_2+M)(1+h_{fe}) - \frac{1}{C}(L_1+L_2+2M)C = 0$$

$$\Rightarrow \quad (L_2+M)(1+h_{fe}) = L_1+L_2+2M$$

$$L_2+M+(L_2+M)(h_{fe}) = L_1+L_2+2M$$

$$(L_2+M)h_{fe} = L_1+M \Rightarrow h_{fe} = \frac{L_1+M}{L_2+M}$$

$\therefore$ The condition for maintenance of oscillations is $\boxed{h_{fe} = \frac{L_1+M}{L_2+M}}$

COLPITTS OSCILLATOR:

In the Colpitt's oscillator Z_1 and Z_2 are capacitors and Z_3 is an inductor. The Colpitt's oscillator circuit is as shown in below fig.

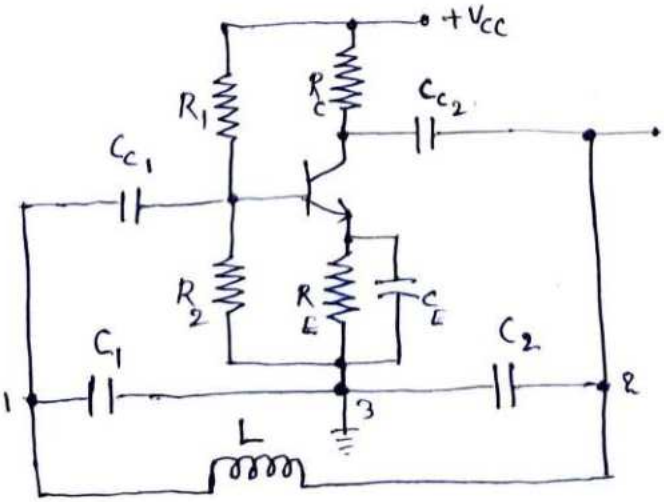


fig: COLPITTS OSCILLATOR

The resistors R_1, R_2 and R_E provide the necessary DC biasing to the transistor. C_E is the bypass capacitor, C_{C_1} and C_{C_2} are the coupling capacitors. The feedback network consists of C_1 and C_2 and an inductor L determines the frequency of oscillation. Here C_1 and C_2 are capacitors.

When the power supply voltage $+V_{CC}$ is switched ON, a transient current is produced in the tank circuit and consequently damped harmonic oscillations are setup in the circuit. The current in the tank circuit produces (or) develops AC voltages across C_1 and C_2. As terminal 3 is grounded, it will be at zero potential. Now if terminal 1 is at positive potential with respect to 3 at any instant, the terminal 2 will be at negative potential with respect to 3 at the same instant. Thus the phase difference between the terminals 1 and 2 is always 180°. In the common emitter configuration, the transistor provides a phase difference of 180° between the input and output. Therefore the total phase difference is 360°. Thus, at the frequency determined for the tank circuit, the necessary condition for sustained oscillations is satisfied. If the feedback is adjusted such that the loop gain $A\beta = 1$, the circuit acts as oscillator. The frequency of oscillation is $f_0 = \frac{1}{2\pi\sqrt{LC}}$

where $\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} \Rightarrow C = \frac{C_1 C_2}{C_1 + C_2}$

It is widely used in commercial signal generators for frequencies between 1MHz to 500MHz. It is also used as a local oscillator in super heterodyne radio receiver.

Analysis: For Colpitts oscillator $Z_1 = \frac{1}{j\omega C_1}$, $Z_2 = \frac{1}{j\omega C_2}$, $Z_3 = j\omega L$

i.e $Z_1 = \frac{-j}{\omega C_1}$, $Z_2 = \frac{-j}{\omega C_2}$ and $Z_3 = j\omega L$

we know the general equation of an LC oscillator is

$$h_{ie}(Z_1+Z_2+Z_3)+Z_1Z_2(1+h_{fe})+Z_1Z_3=0$$

substituting $Z_3=+j\omega L$, $Z_1=\frac{-j}{\omega C_1}$, $Z_2=\frac{-j}{\omega C_2}$ in the above eq'

$$h_{ie}\left(\frac{-j}{\omega C_1}\frac{-j}{\omega C_2}+j\omega L\right)+\left(\frac{-j}{\omega C_1}\cdot\frac{-j}{\omega C_2}\right)(1+h_{fe})+\left(\frac{-j}{\omega C_1}\right)(j\omega L)=0$$

$$-jh_{ie}\left(\frac{1}{\omega C_1}+\frac{1}{\omega C_2}-\omega L\right)-\frac{(1+h_{fe})}{\omega^2 C_1C_2}+\frac{L}{C_1}=0$$

$$\Rightarrow \left[\frac{1+h_{fe}}{\omega^2 C_1C_2}-\frac{L}{C_1}\right]+jh_{ie}\left(\frac{1}{\omega C_1}+\frac{1}{\omega C_2}-\omega L\right)=0 \longrightarrow (1)$$

The frequency of oscillation $f_0=\frac{\omega_0}{2\pi}$ is determined by equating the imaginary part to zero, by substituting $\omega=\omega_0$.

i.e $$h_{ie}\left(\frac{1}{\omega_0 C_1}+\frac{1}{\omega_0 C_2}-\omega_0 L\right)=0$$

$$\Rightarrow \quad \omega_0 L=\frac{1}{\omega_0 C_1}+\frac{1}{\omega_0 C_2}$$

$$\omega_0^2=\frac{1}{L}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)$$

$$\omega_0=\sqrt{\frac{C_1+C_2}{LC_1C_2}} \longrightarrow (2)$$

$$f_0=\frac{\omega_0}{2\pi}=\frac{1}{2\pi}\sqrt{\frac{C_1+C_2}{LC_1C_2}} \longrightarrow (3)$$

The condition for maintenance of oscillation is obtained by substituting equation (3) in equation (1) which makes the imaginary part to zero.

Hence $$\frac{1+h_{fe}}{\omega_0^2 C_1C_2}-\frac{L}{C_1}=0$$

$$\Rightarrow \quad \frac{1+h_{fe}}{\omega_0^2 C_1C_2}=\frac{L}{C_1}$$

$$\Rightarrow \quad \frac{1+h_{fe}}{\left(\frac{C_1+C_2}{LC_1C_2}\right)\cdot C_1C_2}=\frac{L}{C_1} \qquad \left(\because \text{ from eq (2) } \omega_0^2=\frac{C_1+C_2}{LC_1C_2}\right)$$

$$\Rightarrow 1+h_{fe} = \left(\frac{L}{C_1}\right)\left(\frac{C_1+C_2}{L}\right)$$

$$\Rightarrow 1+h_{fe} = \frac{C_1+C_2}{C_1}$$

$$\Rightarrow 1+h_{fe} = 1+\frac{C_2}{C_1}$$

$$\therefore \boxed{h_{fe} = \frac{C_2}{C_1}}$$

Problems: In the Hartley oscillator $L_2 = 0.4\,mH$ and $C = 0.004\,HF$ If the frequency of oscillator is 120kHz, find the value of L_1. Neglect the mutual inductance.

Sol) Given $L_2 = 0.4\,mH = 0.4\times10^{-3}\,H$, $C = 0.004\,HF = 4\times10^{-9}\,F$

$f_0 = 120\,KHz$, $L_1 = ?$

we know that the frequency of Hartley oscillator is given by

$$f_0 = \frac{1}{2\pi\sqrt{(L_1+L_2+2M)C}}$$

Neglecting mutual inductance

$$f_0 = \frac{1}{2\pi\sqrt{(L_1+L_2)C}}$$

$$\Rightarrow f_0^2 = \frac{1}{4\pi^2(L+L_2)C}$$

$$\Rightarrow (L_1+L_2)C = \frac{1}{4\pi^2 f_0^2}$$

$$\Rightarrow L_1C+L_2C = \frac{1}{4\pi^2 f_0^2}$$

$$\Rightarrow L_1C = \frac{1}{4\pi^2 f_0^2} - L_2C$$

$$\Rightarrow L_1 = \frac{1}{4\pi^2 f_0^2 C} - L_2$$

$$\Rightarrow L_1 = \frac{1}{4\pi^2(120\times10^3)^2(4\times10^{-9})} - (0.4\times10^{-3})$$

$$\Rightarrow L_1 = 0.03976\,mH$$

② A Hartley oscillator has two inductances as 2mH and 20μH while the frequency is to be changed from 950KHZ to 2050KHZ Calculate the range over which the capacitor is to be varied.

Sol) Given Hartley oscillator has $L_1 = 2mH = 2\times10^{-3}H$

$L_2 = 20\mu H = 20\times10^{-6}H$, $f_1 = 950KHZ = 950\times10^3 HZ$

$f_2 = 2050KHZ = 2050\times10^3 HZ$.

we know that the frequency of oscillation for hartley oscillator is $f_0 = \frac{1}{2\pi\sqrt{(L_1+L_2)C}}$

$\Rightarrow C = \frac{1}{4\pi^2 f_0^2 (L_1+L_2)}$

when $f_0 = 950KHZ$, $C = \frac{1}{4\pi^2(950\times10^3)^2(2\times10^{-3}+20\times10^{-6})}$

$= 13.89PF$

when $f_0 = 2050KHZ$, $C = \frac{1}{4\pi^2(2050\times10^3)^2(2\times10^{-3}+20\times10^{-6})}$

$C = 2.98PF$

Therefore the range of capacitance is from 2.98PF to 13.89PF.

3) A colpitts oscillator has $C_1 = 0.2PF$ $C_2 = 0.02PF$. If the frequency of oscillation is 10KHZ, find the value of the inductor L?

Sol) Given $C_1 = 0.2PF$, $C_2 = 0.02PF$

$f_0 = 10KHZ$

$L = ?$

we know that the frequency of oscillation for a colpitts oxillator is given by $f_0 = \frac{1}{2\pi\sqrt{L\left(\frac{C_1C_2}{C_1+C_2}\right)}} \Rightarrow f_0^2 = \frac{1}{4\pi^2\left(L\frac{C_1C_2}{C_1+C_2}\right)}$

$$\Rightarrow L = \frac{C_1 + C_2}{4\pi^2 f_0^2 C_1 C_2}$$

$$= \frac{(0.2\times10^{-12}) + (0.02\times10^{-12})}{4\pi^2 \times (10\times10^3)^2 \times 0.2\times10^{-12} \times 0.02\times10^{-12}}$$

$$L = 13931\ H$$

4) In a colpitts oscillator the values of the inductors and capacitors are $L = 40mH$, $C_1 = 100pF$ $C_2 = 500pF$ i) find the frequency of oscillations ii) Find the value of h_{fe} for maintaining sustained oscillations

Sol) Given $L = 40mH$

$C_1 = 100pF$

$C_2 = 500pF$

For a colpitts oscillator the frequency of oscillations is

$$f_0 = \frac{1}{2\pi\sqrt{L\left(\frac{C_1 C_2}{C_1 + C_2}\right)}}$$

$$= \frac{1}{2\pi\sqrt{40\times10^{-3} \times \frac{100\times10^{-12}\times500\times10^{-12}}{(100+500)\times10^{-12}}}}$$

$$\therefore f_0 = 87.172\ KHz$$

ii) The value of h_{fe} for maintaing sustained oscillations in a colpitts oscillator is given by $h_{fe} = \frac{C_2}{C_1}$

$$h_{fe} = \frac{500\times10^{-12}}{100\times10^{-12}}$$

$$\therefore h_{fe} = 5$$

CLAPP OSCILLATOR:

To achieve the frequency stability, colpitts oscillator is slightly modified in practice. This modified colpitts oscillator is called clapp oscillator. In clapp oscillator Z_1 and Z_2 are capacitors and Z_3 is the series combination of an inductor L and a capacitor C_3 as shown in figure below.

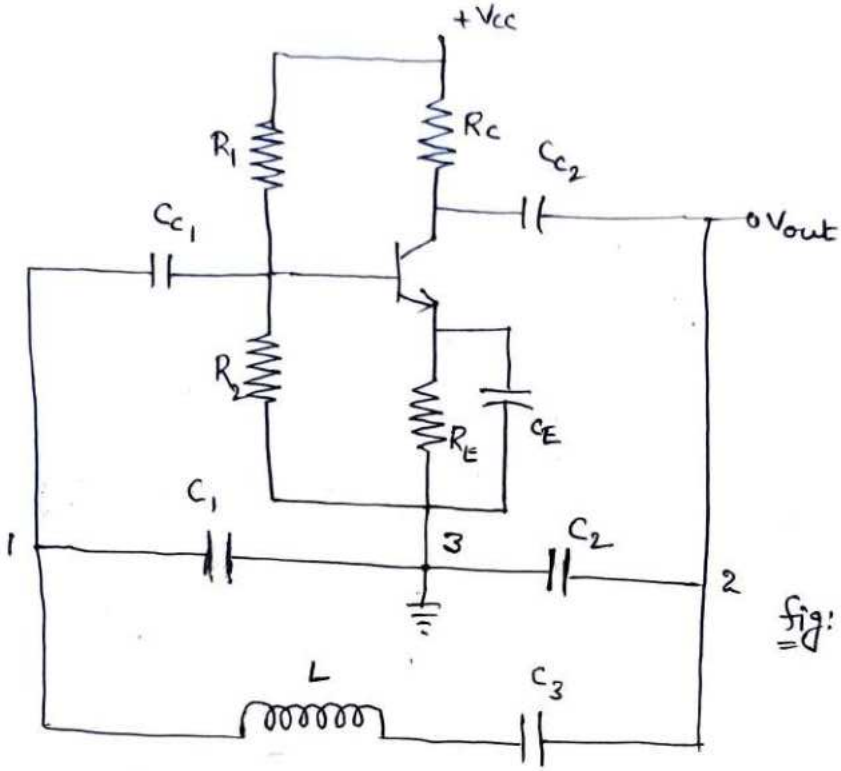


fig: clapp oscillator

The frequency of oscillation for a clapp oscillator is given as

$$f_0 = \frac{1}{2\pi\sqrt{L C_{eq}}}$$

where $\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$. The value of C_3 is very much smaller than the value of C_1 and C_2. So neglecting $\frac{1}{C_1}$ and $\frac{1}{C_2}$ we get

$$\frac{1}{C_{eq}} \simeq \frac{1}{C_3}$$

$$\text{ie } C_{eq} = C_3$$

$$\therefore f_0 = \frac{1}{2\pi\sqrt{L C_3}}$$

The Analysis of a clapp oscillator is as shown in below.

Analysis:

In a Clapp oscillator Z_1 and Z_2 are the capacitive reactances, Z_3 is a series combination of an inductive reactance and a capacitive reactance.

ie $Z_1 = \frac{1}{j\omega C_1} = -\frac{j}{\omega C_1}$

$Z_2 = \frac{1}{j\omega C_2} = -\frac{j}{\omega C_2}$

$Z_3 = j\omega L + \frac{1}{j\omega C_3} = j\omega L - \frac{j}{\omega C_3}$

we know the general equation for an LC oscillator is

$$h_{ie}(Z_1+Z_2+Z_3) + (1+h_{fe})Z_1Z_2 + Z_1Z_3 = 0$$

Substituting Z_1, Z_2, Z_3 in the above equation

$$h_{ie}\left(-\frac{j}{\omega C_1} + \frac{-j}{\omega C_2} + j\omega L + \frac{-j}{\omega C_3}\right) + (1+h_{fe})\left(\frac{-j}{\omega C_1}\right)\left(\frac{-j}{\omega C_2}\right) + \left(\frac{-j}{\omega C_1}\right) \cdot \left(j\omega L - \frac{j}{\omega C_3}\right) = 0$$

$$\Rightarrow -j h_{ie}\left(\frac{1}{\omega C_1} + \frac{1}{\omega C_2} + \frac{1}{\omega C_3} - \omega L\right) - \frac{(1+h_{fe})}{\omega^2 C_1 C_2} + \frac{1}{\omega C_1}\left(\omega L - \frac{1}{\omega C_3}\right) = 0$$

$$\Rightarrow -j h_{ie}\left(\frac{1}{\omega C_1} + \frac{1}{\omega C_2} + \frac{1}{\omega C_3} - \omega L\right) - \frac{1}{\omega C_1}\left[\frac{(1+h_{fe})}{\omega C_2} - \omega L + \frac{1}{\omega C_3}\right] = 0$$

The frequency of oscillation $f_0 = \frac{\omega_0}{2\pi}$ can be determined by equating the imaginary part to zero.

$$-h_{ie}\left(\frac{1}{\omega_0 C_1} + \frac{1}{\omega_0 C_2} + \frac{1}{\omega_0 C_3} - \omega_0 L\right) = 0$$

$$\Rightarrow \frac{1}{\omega_0 C_1} + \frac{1}{\omega_0 C_2} + \frac{1}{\omega_0 C_3} - \omega_0 L = 0$$

$$\Rightarrow \frac{1}{\omega_0}\left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}\right) = \omega_0 L$$

$$\Rightarrow \omega_0^2 = \frac{1}{LC_{eq}} \quad \text{where } \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} = \frac{1}{C_{eq}}$$

$$\Rightarrow \omega_0 = \frac{1}{\sqrt{L C_{eq}}}$$

$$\Rightarrow f_0 = \frac{1}{2\pi\sqrt{L C_{eq}}}$$

where $\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$

As C_3 is very much smaller than C_1 and C_2. We can neglect $\frac{1}{C_1}$ and $\frac{1}{C_2}$.

$$\therefore \frac{1}{C_{eq}} \simeq \frac{1}{C_3}$$

$$\Rightarrow C_{eq} = C_3$$

$\therefore$ the frequency of oscillation for Clapp oscillator is

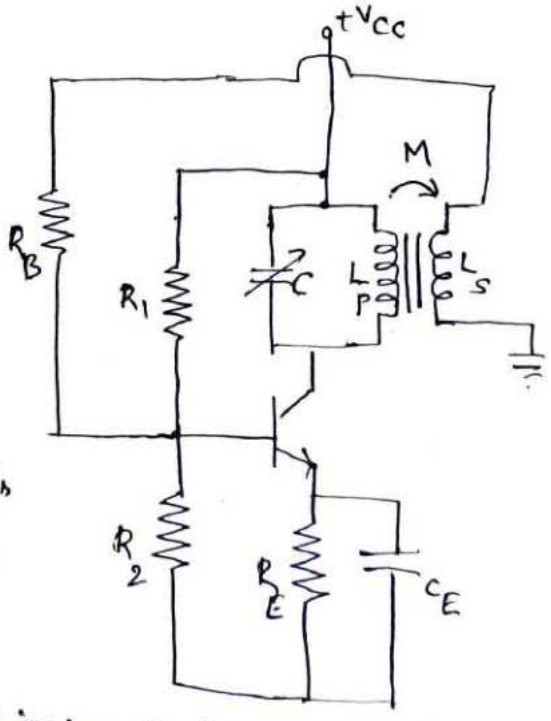
$$\boxed{f_0 = \frac{1}{2\pi\sqrt{LC_3}}}$$

Advantages:

1) The frequency is stable and accurate
2) The stray capacitances have no effect as C_3 decides the frequency.
3) Keeping C_3 variable, the frequency can be varied in the desired range.

Tuned collector oscillator:

A tuned collector oscillator circuit is as shown in figure. There is a tuned LC circuit in the collector branch, which is connected to power supply $+V_{CC}$. Resistors R_1, R_2 and R_E are used to establish the proper biasing conditions as in a common emitter amplifier.



The capacitor C_E is a bypass emitter capacitor. The resistor R_B is used to control the amount of feedback to the value just needed for sustained oscillation.

When the power supply is switched on, the capacitor C starts charging. When it is fully charged, it starts to discharge through L_p. The energy stored in capacitor 'C' is in the form of electrostatic energy which gets converted to electromagnetic energy and gets stored in L_p. Once the capacitor discharges completely, L_p starts charging capacitor again. So the capacitor starts charging again and this cycle continues.

The coil L_s gets charged through the electromagnetic induction and feeds this to the transistor. The transistor amplifies the signal and is taken as the output at collector. A part of the output is fed back to the base through the LC circuit present at collector with positive feedback.

Here, the common Emitter amplifier introduces 180° phase shift and the transformer introduces an additional 180° phase shift hence a total 360° phase shift is obtained which satisfies the desired condition for sustained oscillations.

The frequency of oscillation $f_0 = \frac{1}{2\pi\sqrt{L_p C}}$

Drawbacks of LC oscillators:

1) Frequency instability
2) Waveform is poor
3) It cannot be used for deriving low frequencies.
4) Inductors are bulky and inexpensive.

Frequency Stability of oscillator:

↱ The frequency of oscillations should remain constant. But practically the frequency of oscillations will get changed due to various reasons.

↱ The analysis of the dependence of the oscillating frequency on various factors like temperature, internal capacitance etc is called as "frequency stability analysis."

↱ The measure of ability of an oscillator to maintain the desired frequency as precisely as possible for as long time as possible is called as the "frequency stability".

↱ The transistor parameters are temperature sensitive. Hence as temperature changes, the oscillating frequency also changes and no longer remains stable. So the circuit cannot provide stable frequency.

Factors that affect the frequency stability:

1) The operating point of the active devices such as BJT and FET must be in the active region. Due to the change in temperature the parameters of the active devices like BJT, FET may get changed that may lead to the change in frequency of oscillation.

2) The circuit components that are temperature dependent may affect the frequency of oscillation.

3) The changes in the DC supply voltage applied in the circuit may shift the oscillator's frequency of oscillation.

4) The changes in the atmospheric conditions and aging of the components may affect the frequency of oscillation.

5) The internal capacitances of the transistor may affect the oscillator's frequency of oscillation.

6) The changes in the output load / output resistance that may cause a change in the Q-factor of the tank circuit, thereby causing a change in the frequency oscillation.

The variation of frequency with respect to temperature variation is given by $S_{\omega,T} = \frac{\Delta\omega/\omega_0}{\Delta T/T_0}$ (ppmc Parts per million - per °C)

where ω_0 = The desired frequency of oscillation

T_0 = operating temperature

The frequency stability is debined as $S_\omega = \frac{d\theta}{d\omega}$

where θ is the phase shift which introduced due to the variation in the desired frequency (f_0).

The circuit should have $\frac{d\theta}{d\omega}$ as large as possible to have more frequency stability.

Amplitude Stability:

The ability of an oscillator to maintain a constant amplitude in the output waveform for as long time as possible is called as the amplitude stability of the oscillator.

The amplitude against the variations due to aging of the components can be stabilized by replacing the resistors in bridge by sensistors which are temperature dependent resistors.

All the oscillators donot require positive feedback for their operation. If the positive resistance of the LC tank circuit is cancelled by introducing the right amount of -ve resistance across the tank circuit.

There are several devices that exhibit negative resistance such as dynatron, transitron, thermistor, UJT and tunnel diode, with in a particular region in their V-I characteristics. Such devices are operated under that negative resistance region and they are placed in the tank circuit to cancel the positive resistance of the tank circuit.

The negative resistance should be numerically less than the dynamic resistance of the tuned circuit.

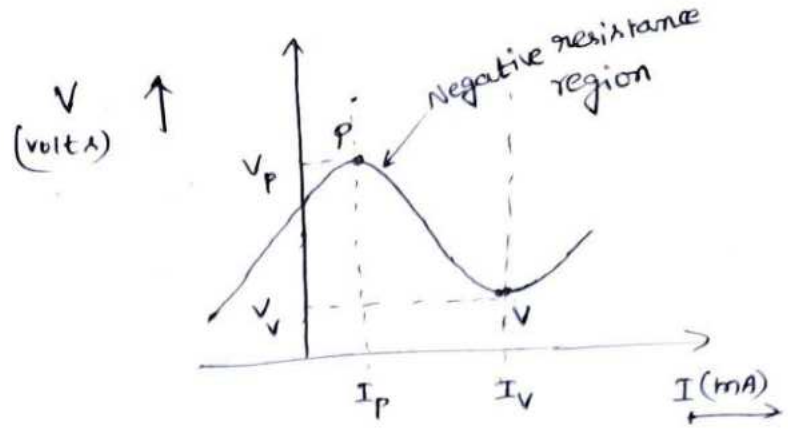


fig: V-I characteristics of negative resistance device

Crystal oscillators:

The following figure shows a crystal controlled oscillator. Here a colpitts oscillator is taken in which the inductor is replaced by a crystal. The crystal should be a piezo electric crystal usually quartz is used as a resonant circuit.

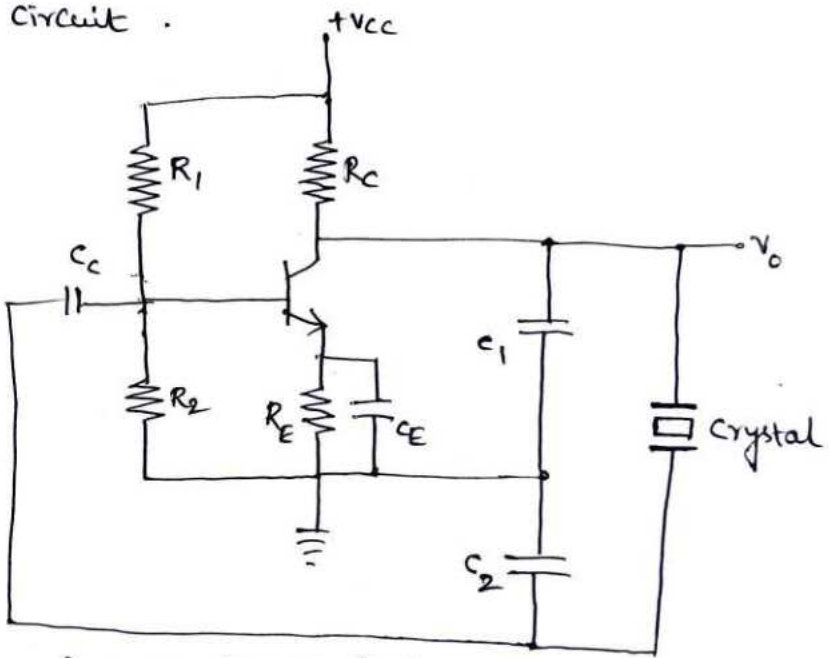


figure: Crystal Controlled oscillator.

Principle of operation:

A crystal is a thin slice of piezo electric material such as quartz, tourmaline and rochelle salt which exhibit a property called piezo - electric effect.

Piezo electric effect means under the influence of the mechanical pressure on one face of the crystal, an ac voltage is developed across the opposite faces of the crystal. Conversely if the a.c - voltage is applied across two opposite faces, it causes a mechanical vibration in the crystal.

Quartz Crystal Construction:

Generally the crystal is a ground wafer of quartz or tourmaline stone placed between two metal plates. The crystal is placed after cutting crude crystal wafer into slices.

There are two methods of cutting the crystal. Based on the method of cutting the resonant frequency of the crystal and it's temperature coefficient is decided.

When the crystal wafer is cut in such a way that it's flat surfaces are perpendicular to it's electrical axis (X-axis), it is called as an X-Cut Crystal.

When the crystal wafer is cut in such a way that it's flat surfaces are perpendicular to it's mechanical axis (Y-axis), it is called as a Y-Cut Crystal.

If an AC voltage is applied, the crystal is set into vibration. The frequency of vibration is equal to the resonant frequency of the crystal. Usually the resonant frequency of the crystal is determined by the structural characteristics of the crystal. If the frequency of the applied AC voltage is equal to the natural resonant frequency of the crystal the vibration will be obtained with maximum amplitude.

In general the frequency of the vibration is given by

$$f = \frac{p}{2l}\sqrt{\frac{Y}{\rho}}$$

where $p = 1, 2, 3 \cdots$, Y is the young modulus,

ρ = density of the material

l = length of the material.

The crystal is suitably cut to get the vibrations with the required frequency and is mounted between two metal plates as shown in figure (a). The equivalent circuit of the crystal is

as shown in figure (b).

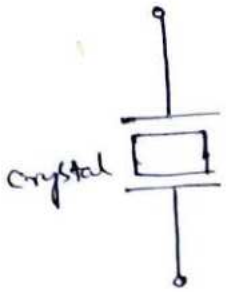
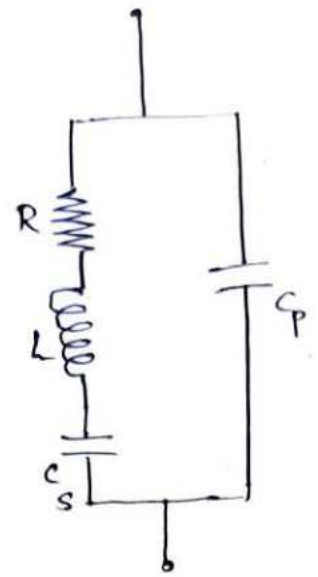


fig (a) Symbol of a Piezo electric crystal



fig(b) Equivalent circuit of a crystal

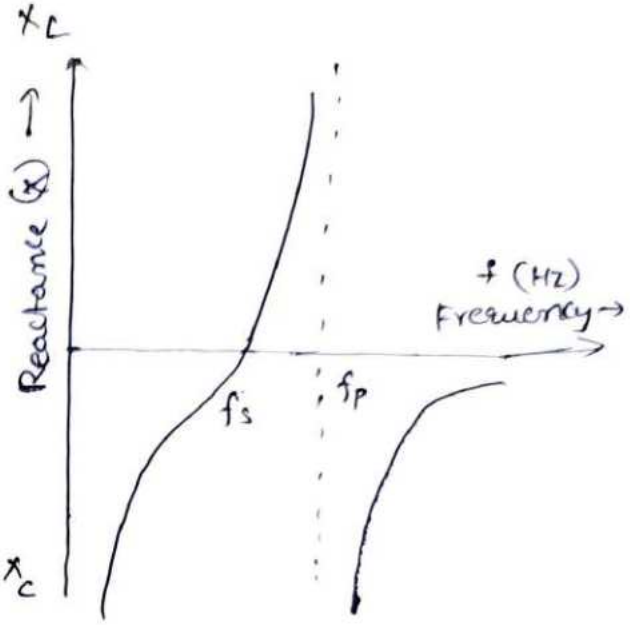


fig: reactance function with respect to frequency when R=0.

The reactance of the crystal is given by the formula

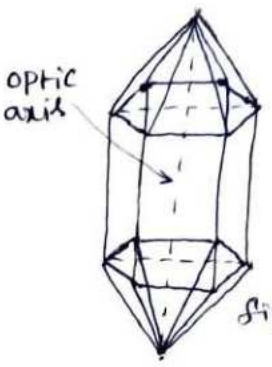
$$jX = \frac{1}{j\omega C_p} \cdot \left(\frac{\omega^2 - \omega_s^2}{\omega^2 - \omega_p^2} \right) \text{ (neglecting R).}$$

Here ω_s = series resonant frequency $= \frac{1}{\sqrt{LC_s}}$

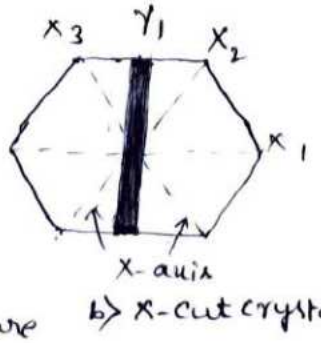
ω_p = parallel resonant frequency $= \frac{1}{\sqrt{L\left(\frac{C_s C_p}{C_s + C_p}\right)}}$

If C_p is very much larger than C_s then the parallel resonant frequency will be approximately equal to series resonant frequency.

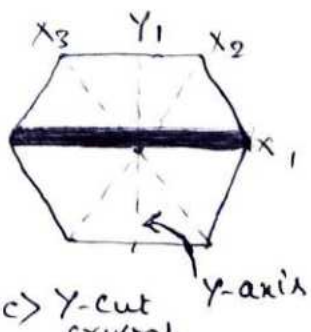
The structure of the Quartz crystal and the crystal wafer cutting, using X-cut and Y-cut are as shown in below.



fig(a): Quartz Crystal structure



b) X-cut crystal



c) Y-cut crystal

series resonant frequency is the frequency at which reactance of the inductance L is equal to the reactance of the capacitance C_s. In this case the impedance of the equivalent circuit is equal to resistance 'R'.

The Parallel resonant frequency is the frequency at which the reactance of the RLC branch is equal to the reactance of the capacitor C_p.

Advantages of Crystal oscillator:

1) Crystal oscillator offers very high frequency stability.
2) Crystal oscillator circuits are less expensive
3) Quartz crystal has small size and light weight, which is preferred in crystal oscillator.
4) Crystals also have very high quality factor (Q).
5) It also provides good temperature stability.

Disadvantages of Crystal oscillator:

1) Crystals are very delicate and fragile, so they should be handled carefully.
2) The increase in the frequency, decreases the thickness of the crystal. This inturn reduces the mechanical strength of the crystal.
3) Crystal oscillators have fixed frequency of oscillation. Therefore, for every frequency of oscillation, the entire circuit must be redesigned.
4) The crystal oscillators are used only in low power circuits.

Problem

A crystal has L = 2H, C = 0.01PF and R = 2KΩ. It has a mounting capacitance of 2PF. Calculate it's series and parallel resonant frequencies.

Sol) Given $L = 2H$, $C = C_s = 0.01PF$, $R = 2K\Omega$

Mounting capacitance $C_p = 2PF$

series resonant frequency $f_s = \frac{1}{2\pi\sqrt{LC_s}} = \frac{1}{2\pi\sqrt{2 \times 0.01 \times 10^{-12}}} = 1.12MHz$

Parallel resonant frequency $f_p = \frac{1}{2\pi\sqrt{\frac{L C_s C_p}{C_s + C_p}}}$

$$\Rightarrow f_p = \frac{1}{2\pi\sqrt{\frac{2 \times 0.01\times10^{-12} \times 2\times10^{-12}}{(0.01+2)\,10^{-12}}}}$$

$$\therefore f_p = 1.13\,MHz$$

Note: In the above problem $f_s \simeq f_p$ as the values of C_s and C_p are such that $C_p >> C_s$.

2) A crystal has $L = 0.5H$, $C_s = 0.06PF$, $C_p = 1PF$, $R = 5K\Omega$. Find the series and parallel resonant frequency and Q-factor of the crystal at series resonance and parallel resonance.

Sol) Given $L = 0.5H$, $C_s = 0.06PF$, $C_p = 1PF$, $R = 5K\Omega$

series resonant frequency $f_s = \frac{1}{2\pi\sqrt{LC_s}}$

$$= \frac{1}{2\pi\sqrt{(0.5)(0.06\times10^{-12})}}$$

$$\therefore f_s = 918.9\,KHz$$

Q-factor at series resonance is $Q_s = \frac{\omega_s L}{R}$

$$\Rightarrow Q_s = \frac{2\pi f_s L}{R} = \frac{2\pi \times 918.9\times10^{3} \times 0.5}{5\times10^{3}}$$

$$\Rightarrow Q_s = 577$$

Parallel resonant frequency $f_p = \frac{1}{2\pi\sqrt{\frac{L C_s C_p}{C_s + C_p}}}$

$$\Rightarrow f_p = \frac{1}{2\pi\sqrt{(0.5)\left(\frac{0.06\times10^{-12} \times 1\times10^{-12}}{(0.06+1)\times10^{-12}}\right)}}$$

$$\Rightarrow f_p = 946\,KHz$$

Q-factor at parallel resonance is $Q_p = \frac{\omega_p L}{R} = \frac{2\pi f_p L}{R}$

$$\Rightarrow Q_p = \frac{2\pi \times (946\times10^{3}) \times 0.5}{5\times10^{3}} = 594$$

Pierce Crystal oscillator:

The transistor pierce crystal oscillator is as shown in below figure.

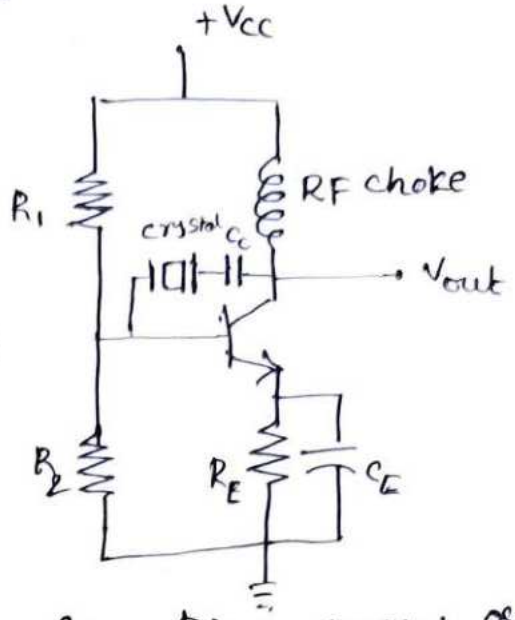


fig: Pierce crystal oscillator

Here the crystal is connected in the feed back path from collector to base.

The resistors R_1, R_2 and R_E are used to establish proper biasing in the circuit.

The RF choke used in the circuit, is for isolation of ac and dc.

C_c is the coupling capacitance. C_E is the emitter bypass capacitor which is used to prevent the amplification loses.

The coupling capacitor C_c blocks the dc voltage between the collector and base and it has a negligible impedance at the frequency of the oscillator.

The frequency of oscillation set by the series resonant frequency of the crystal is given by

$$f_o = \frac{1}{2\pi\sqrt{LC_s}}$$

The main advantage of the pierce crystal oscillator is it's simplicity.

It is the most frequently used crystal oscillator.

→ A tuned collector oscillator in a radio receiver has a fixed inductance of 60μH and has to be tunable over the frequency band of 400 KHz to 1200KHz. find the range of capacitor to be used.

sol> Given $L_p = 60\mu H$, $f_{min} = 400KHz$, $f_{max} = 1200KHz$

Frequency of oscillation for tuned collector oscillator is

$$f_o = \frac{1}{2\pi\sqrt{L_p C}}$$. At $f = f_{min}$, capacitance $C = C_{max}$

$$\Rightarrow C_{max} = \frac{1}{4\pi^2 f_{min}^2 L_p} = \frac{1}{4\pi^2 (400\times10^3)^2 (60\times10^{-6})} = 2641\,PF$$

At $f = f_{max}$ capacitance $C = C_{min}$

$$\therefore C_{min} = \frac{1}{4\pi^2 f_{max}^2 \cdot L_p} = \frac{1}{4\pi^2 (1200\times10^3)^2 \cdot (60\times10^{-6})}$$

$$\Rightarrow C_{min} = 293PF$$

∴ The range of the capacitor is 293 PF - 2641 PF.

→ Design a hartley oscillator that generates the frequency of oscillation at 1 MHz.

sol> In a hartley oscillator the tank circuit contains two inductors L_1 and L_2 and a capacitor C which decides the frequency of oscillation $f_o = \frac{1}{2\pi\sqrt{(L_1+L_2+2M)C}}$ → (1)

Let the mutual inductance $M = 0$.

Let us assume $C = 500pF$

Given frequency of oscillation $f_o = 1MHz = 1\times10^6 Hz$

Substituting $M=0$ in equation (1) we get

$$f_o = \frac{1}{2\pi\sqrt{(L_1+L_2)C}}$$

$$\Rightarrow f_0^2 = \frac{1}{4\pi^2 (L_1+L_2) C}$$

$$\Rightarrow L_1+L_2 = \frac{1}{4\pi^2 f_0^2 C} = \frac{1}{4\pi^2 (1\times10^6)^2 \times 500\times10^{-12}}$$

$$\Rightarrow L_1+L_2 = 5.066\times10^{-5} = 50.66\,\mu F \simeq 50\,\mu F$$

Let $L_1 = 32\,\mu F$ and $L_2 = 18\,\mu F$ such that the sum of L_1 and L_2 is $50\,\mu F$.

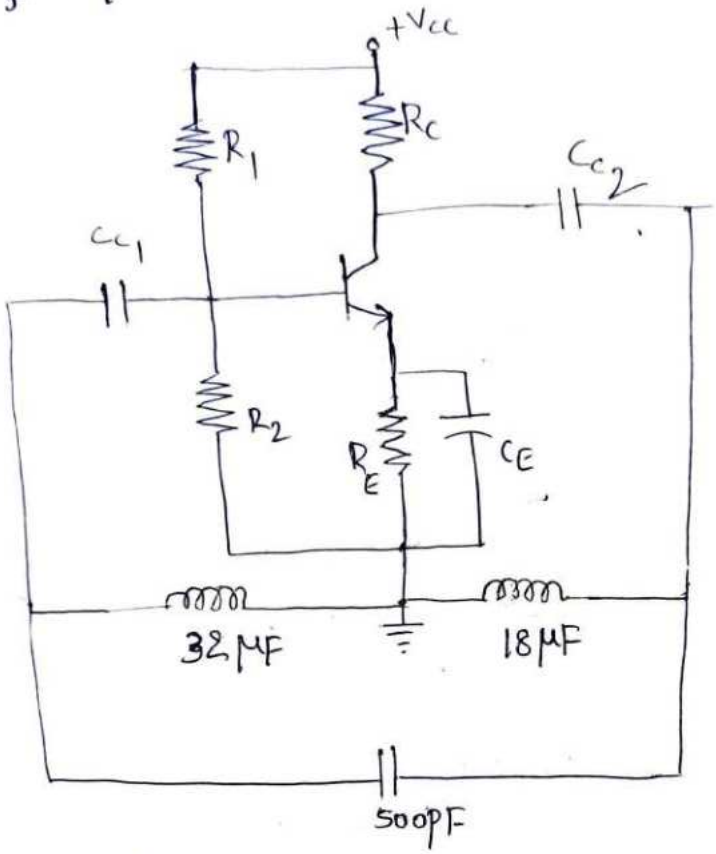


fig: Hartley oscillator

H.W Design a colpitt's oscillator that generates a signal with frequency of oscillation at 1MHz.

→ Find the value of h_{fe} to satisfy the condition for frequency of a signal (f_0) with sustained oscillations for a hartley oscillator having $L_1 = 10\,\mu F$, $L_2 = 2\,\mu F$ and $C = 5\,pF$. Assume $M = 0$.

sol) To get sustained oscillation in hartley oscillator the condition for $h_{fe} = \frac{L_1}{L_2} = \frac{10\times10^{-6}}{2\times10^{-6}} = 5$

RC Oscillators :

All the LC oscillators are very useful to generate the signals with high frequencies. But the low frequency signals are generated with higher values of inductance and capacitances. This leads the circuit to be bulky and infact the circuit becomes expensive. The signals of low frequencies are easily generated with RC - oscillators.

RC oscillators are mainly of two types.

i) RC Phase shift oscillator ii) Wien bridge oscillator.

i) RC phase shift oscillator using cascade Connection of Highpass filter:

In this oscillator the required phase shift of 180° in the feedback loop from output to input is obtained by using R and C components instead of tank circuit.

The following figure shows the circuit of RC Phase shift oscillator using cascade connection of high pass filter.

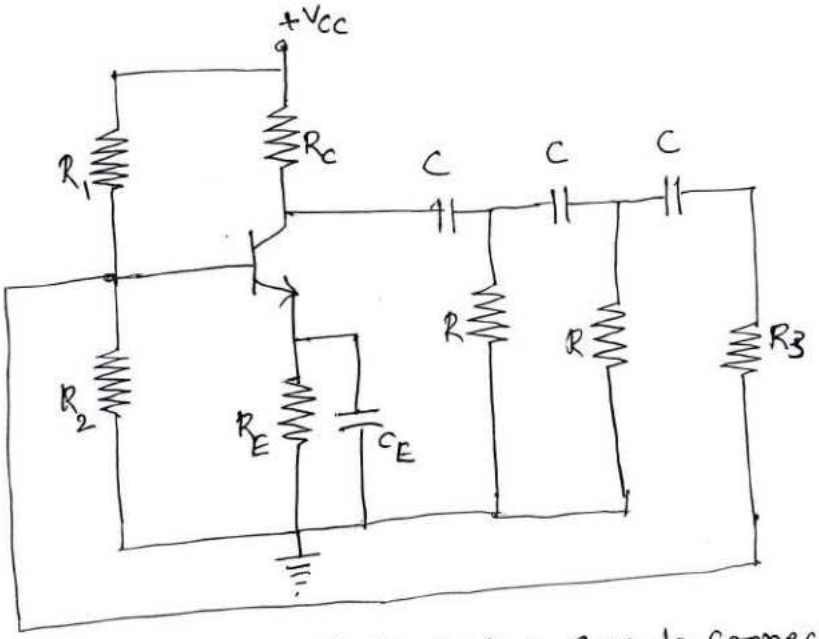


fig a) RC Phaseshift oscillator using cascade connection of High pass filter.

Here a common Emitter amplifier is followed by three sections of RC phase shift network. The output of the last section is connected as the input to the base of the transistor.

In order to make the three RC sections identical, R_3 is selected such that $R_3 + R_i = R$, where R_i is the input impedance of circuit.

Since the BJT is connected in CE configuration the input impedance R_i is equal to h_{ie}. That means $R_3 + h_{ie} = R$, neglecting R_1 & R_2.

The phase shift of each RC section is given by

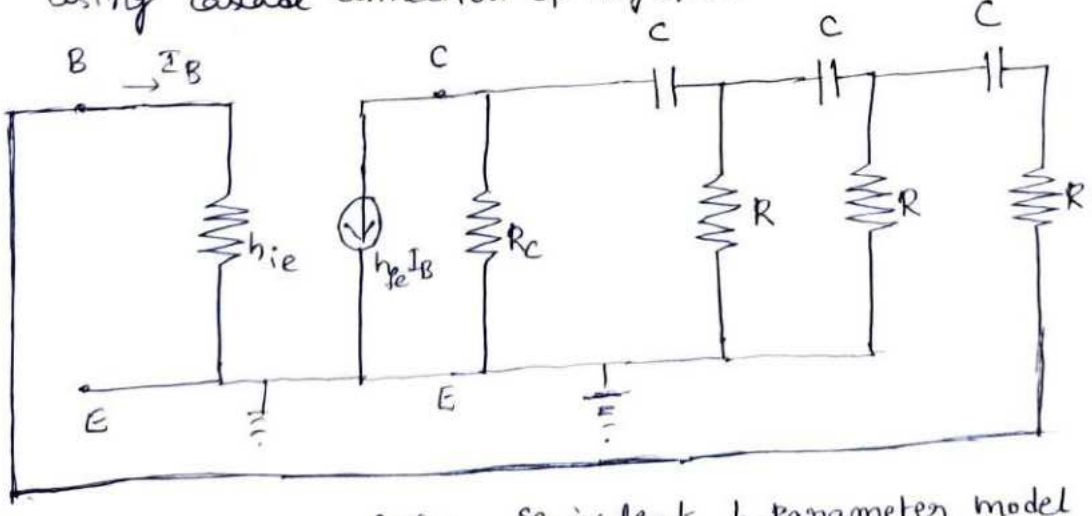
$$\phi = \tan^{-1}\left(\frac{1}{\omega CR}\right)$$

If R and C values are chosen such that for a given frequency f_r, the phase shift of each RC section is 60°. Thus the RC ladder network produces a total phase shift of 180°, between it's input and output voltages for the given frequency. The transistor of CE configuration provides a phase shift of 180°. Therefore a total phase shift of 360° is obtained, that satisfies the condition for sustained oscillations ie satisfying Barkhausen criterion. For RC phase shift oscillator the frequency of oscillation is given by $f_o = \frac{1}{2\pi RC\sqrt{6+4K}}$ where $K = \frac{R_c}{R}$.

At this frequency, it is found that the feedback factor β is $|\beta| = \frac{1}{29}$.

To get $|A\beta|$ not less than unity the transistor amplifier gain $|A|$ must be greater than or equal to 29.

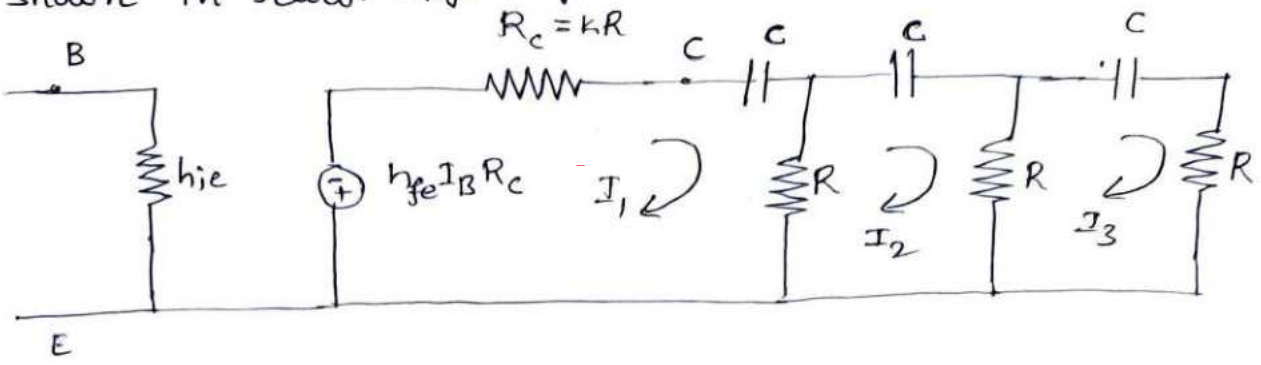
The equivalent h-parameter model for the RC phase shift oscillator using cascade connection of high pass filter is as shown in below.



fig(b) Equivalent h-parameter model

Analysis:

The h-parameter equivalent model for RC phase shift oscillator using cascade connection of highpass filter is modified as shown in below. Neglecting R_1 and R_2 input impedance $R_i \simeq h_{ie}$.



Here we have replaced $R_3 + h_{ie}$ with R and the current source $h_{fe} I_B$ is replaced by it's equivalent voltage source. Assume the ratio of the resistance R_c to R as k. i.e $k = \frac{R_c}{R}$

Applying KVL for loop1 we get

$$I_1 R_C + I_1 \frac{1}{j\omega C} + I_1 R - I_2 R = -h_{fe} I_B R_C$$

Replacing R_c with kR and $j\omega$ by s we get

$$I_1 kR + I_1 \frac{1}{s \cdot C} + I_1 R - I_2 R = -h_{fe} I_B kR$$

$$\Rightarrow \quad I_1 \left[(k+1)R + \frac{1}{sC} \right] - I_2 R = -h_{fe} I_B kR \longrightarrow (1)$$

Applying KVL for loop2 we get

$$I_2 \frac{1}{j\omega C} + I_2 R - I_3 R + I_2 R - I_1 R = 0$$

Replace $j\omega$ by s

$$I_2 \frac{1}{sC} + 2I_2 R - I_3 R - I_1 R = 0$$

$$\Rightarrow \quad -I_1 R + I_2 \left(2R + \frac{1}{sC} \right) - I_3 R = 0 \longrightarrow (2)$$

Apply KVL for loop3 we get

$$I_3 \left(\frac{1}{j\omega C} \right) + I_3 R + I_3 R - I_2 R = 0$$

Replace 'jw by s;

$$\frac{I_3}{sC} + 2I_3R - I_2R = 0$$

$$\Rightarrow \quad -I_2R + I_3\left(2R + \frac{1}{sC}\right) = 0 \longrightarrow (3)$$

using Cramer's rule to solve for I_3

$$D = \begin{vmatrix} (k+1)R + \frac{1}{sC} & -R & 0 \\ -R & 2R + \frac{1}{sC} & -R \\ 0 & -R & 2R + \frac{1}{sC} \end{vmatrix}$$

$$\Rightarrow \quad D = \left[(k+1)R + \frac{1}{sC}\right] \cdot \left[\left(2R + \frac{1}{sC}\right)^2 - R^2\right] - (-R)\left[(-R)\left(2R + \frac{1}{sC}\right) - 0\right] + 0\,(R^2)$$

$$D = \left[(k+1)R + \frac{1}{sC}\right]\left(2R + \frac{1}{sC}\right)^2 - \left[(k+1)R + \frac{1}{sC}\right] \cdot R^2 - R^2\left(2R + \frac{1}{sC}\right) \longrightarrow (4)$$

The first term in the above equation is

$$\left[(k+1)R + \frac{1}{sC}\right]\left(2R + \frac{1}{sC}\right)^2 = \left[\frac{(k+1)RSC + 1}{sC}\right]\left(\frac{2RSC + 1}{s^2C^2}\right)^2$$

$$= \frac{(kRSC + RSC + 1)(4R^2s^2C^2 + 4RSC + 1)}{s^3C^3}$$

$$= \frac{4kR^3s^3C^3 + 4kR^2s^2C^2 + kRSC + 4R^3s^3C^3 + 4R^2s^2C^2 + RSC + 4R^2s^2C^2 + 4RSC + 1}{s^3C^3}$$

$$= \frac{R^3s^3C^3(4k+4) + R^2s^2C^2(4k+8) + RSC(k+5) + 1}{s^3C^3}$$

The second and third terms in equation (4) are combinely written as

$$-\left[(k+1)R + \frac{1}{sC}\right]R^2 - R^2\left(2R + \frac{1}{sC}\right) = -\frac{[(k+1)RSC + 1]R^2}{sC} - \frac{R^2(2RSC+1)}{sC}$$

$$= \frac{-kR^3SC - R^3SC - R^2 - 2R^3SC - R^2}{SC}$$

$$= \frac{-kR^3SC - 3R^3SC - 2R^2}{SC}$$

$$= -\frac{(kR^3SC + 3R^3SC + 2R^2)}{SC}$$

Combining the first term equivalent and second & third term equivalent of equation (4) we get

$$D = \frac{R^3S^3C^3(4k+4) + R^2S^2C^2(4k+8) + RSC(k+5) + 1}{S^3C^3} - \frac{(kR^3SC + 3R^3SC + 2R^2)}{SC}$$

$$\Rightarrow D = \frac{R^3S^3C^3(4k+4) + R^2S^2C^2(4k+8) + RSC(k+5) + 1 - S^2C^2(kR^3SC + 3R^3SC + 2R^2)}{S^3C^3}$$

$$= \frac{R^3S^3C^3(4k+4) + R^2S^2C^2(4k+8) + RSC(k+5) + 1 - kR^3S^3C^3 - 3R^3S^3C^3 - 2R^2S^2C^2}{S^3C^3}$$

$$D = \frac{R^3S^3C^3(3k+1) + R^2S^2C^2(4k+6) + RSC(k+5) + 1}{S^3C^3} \longrightarrow (5)$$

Now

$$D_3 = \begin{vmatrix} (k+1)R + \frac{1}{SC} & -R & -h_{fe}I_BKR \\ -R & 2R + \frac{1}{SC} & 0 \\ 0 & -R & 0 \end{vmatrix}$$

$$= 0 - 0 + (-h_{fe}I_BkR)\cdot(R^2 - 0)$$

$$D_3 = -kR^3h_{fe}I_B \longrightarrow (6)$$

$$\therefore I_3 = \frac{D_3}{D} = \frac{-kR^3h_{fe}I_BS^3C^3}{R^3S^3C^3(3k+1) + R^2S^2C^2(4k+6) + RSC(k+5) + 1} \longrightarrow (7)$$

$(\because$ from equation (5) and (6))

I_3 = output current of the feedback circuit

I_B = Input current of the amplifier

$I_C = h_{fe} I_B$ = Input current of the feedback circuit

Amplifier gain $A = \frac{\text{output of the amplifier}}{\text{Input to the amplifier}} = \frac{I_3}{I_B} = h_{fe}$

Loop gain $A\beta = \frac{I_3}{I_B} \cdot \frac{I_3}{I_C} = h_{fe} \cdot \frac{I_3}{h_{fe} I_B} = \frac{I_3}{I_B}$ ⟶ (8)

$\left(\because \beta = \text{feed back factor} = \frac{\text{output of feedback circuit}}{\text{Input to feedback circuit}} = \frac{I_3}{I_C} \right)$

From equation (7) and (8)

$$A\beta = \frac{I_3}{I_B} = \frac{-KR^3 h_{fe} s^3 c^3}{R^3 s^3 c^3 (3K+1) + R^2 s^2 c^2 (4K+6) + RSC(K+5) + 1} \rightarrow (9)$$

Substituting $s = j\omega$, $s^2 = j^2\omega^2 = -\omega^2$, $s^3 = j^3\omega^3 = -j\omega^3$ in the above equation we get

$$A\beta = \frac{+j\omega^3 KR^3 h_{fe} c^3}{-j\omega^3 R^3 c^3 (3K+1) - \omega^2 R^2 c^2 (4K+6) + j\omega RC(K+5) + 1}$$

$$= \frac{K h_{fe}}{\frac{-j\omega^3 R^3 c^3 (3K+1)}{j\omega^3 R^3 c^3} - \frac{\omega^2 R^2 c^2 (4K+6)}{j\omega^3 R^3 c^3} + \frac{j\omega RC(K+5)}{j\omega^3 R^3 c^3} + \frac{1}{j\omega^3 R^3 c^3}}$$

$$= \frac{K h_{fe}}{-(3K+1) + j\frac{(4K+6)}{\omega RC} + \frac{K+1}{\omega^2 R^2 c^2} - \frac{j}{\omega^3 R^3 c^3}}$$

$$A\beta = \frac{K h_{fe}}{-(3K+1) + j(4K+6)\alpha + (K+5)\alpha^2 - j\alpha^3} \quad \left(\text{where } \alpha = \frac{1}{\omega RC}\right)$$

$$\Rightarrow A\beta = \frac{K h_{fe}}{\left[K\alpha^2 + 5\alpha^2 - 3K - 1\right] + j\left(-\alpha^3 + 4K\alpha + 6\alpha\right)} \rightarrow (10)$$

As per Barkhausen criterion to get sustained oscillations $\angle A\beta = 0^\circ$ (or) 360°. To get $\angle A\beta = 0^\circ$, the imaginary part of the denominator should be 0.

$$\therefore \quad -\alpha^3 + 4k\alpha + 6\alpha = 0$$

$$\Rightarrow \quad \alpha(-\alpha^2 + 4k + 6) = 0$$

$$\Rightarrow \quad -\alpha^2 + 4k + 6 = 0$$

$$\Rightarrow \quad \alpha = \sqrt{4k+6}$$

Replacing $\alpha = \frac{1}{\omega_0 RC}$

$$\frac{1}{\omega_0 RC} = \sqrt{4k+6}$$

$$\omega_0 = \frac{1}{RC\sqrt{4k+6}}$$

$$\therefore \boxed{f_0 = \frac{1}{2\pi RC\sqrt{4k+6}}}$$

This is the frequency at which $\angle A\beta = 0^\circ$. At the same frequency $|A\beta| = 1$, substituting $\alpha = \sqrt{4k+6}$ in equation (10) we get

$$A\beta = \frac{k h_{fe}}{k(4k+6) + 5(4k+6) - 3k - 1}$$

$$= \frac{k h_{fe}}{4k^2 + 6k + 20k + 30 - 3k - 1}$$

$$= \frac{k h_{fe}}{4k^2 + 23k + 29}$$

Now $|A\beta| = 1$

$$\Rightarrow \left| \frac{k h_{fe}}{4k^2 + 23k + 29} \right| = 1 \quad \Rightarrow k h_{fe} = 4k^2 + 23k + 29$$

$$\Rightarrow \boxed{h_{fe} = 4k + 23 + \frac{29}{k}}$$

Minimum value of h_{fe} for the oscillations (or) minimum gain for sustained oscillations:

we know that $h_{fe} = 4K + 23 + \frac{29}{K}$ $\longrightarrow$ (11)

To get minimum value of h_{fe} we have to find $\frac{dh_{fe}}{dK}$ and equate it to zero, in order to get the value of K.

$$\frac{dh_{fe}}{dK} = 4 + 0 + \left(\frac{29}{K^2}\right) = 0$$

$$\Rightarrow \quad 4 - \frac{29}{K^2} = 0$$

$$\Rightarrow \quad K^2 = \frac{29}{4}$$

$$\Rightarrow \quad K = 2.6925$$

$\therefore$ $K = 2.6925$ for minimum h_{fe}

substituting this in equation (11) we get

$$h_{fe_{min}} = 4(2.6925) + 23 + \frac{29}{2.6925}$$

$$\therefore \quad h_{fe_{min}} = 44.54$$

Therefore the minimum gain for sustained oscillations in an RC-Phase shift oscillator is $h_{fe\,min} = 44.54$.

Problem Find the capacitor C and h_{fe} for the transistor to provide the frequency of 10KHz of a transistorized Phase shift oscillator. Assume $R_1 = 25K\Omega$, $R_2 = 57K\Omega$, $R_c = 20K\Omega$, $R = 7.1K\Omega$, and $h_{ie} = 1.8K\Omega$.

Sol) Given $f_o = 10KHz$, $R_1 = 25K\Omega$, $R_2 = 57K\Omega$, $h_{ie} = 1.8K\Omega$, $R = 7.1K\Omega$

Input impedance $Z_i = h_{ie} = 1.8K\Omega$

$$Z_i' = Z_i \,||\, R_1 \,||\, R_2 = 1.8K\Omega \,||\, 25K\Omega \,||\, 57K\Omega = 1.631K\Omega$$

$$R_3 + Z_i' = R \Rightarrow R_3 = R - Z_i' = 7.1K\Omega - 1.631K\Omega = 5.469K\Omega$$

$$K = \frac{R_c}{R} = \frac{20\times10^3}{7.1\times10^3} = 2.8169$$

$$\therefore f = \frac{1}{2\pi RC\sqrt{6+4K}} \Rightarrow 10\times10^3 = \frac{1}{2\pi \times 7.1\times10^3 \times C\sqrt{6+4(2.8169)}}$$

$$\Rightarrow \quad C = \frac{1}{2\pi \times 7.1\times10^{3} \times 10\times10^{3}\sqrt{6+11.2676}}$$

$$\therefore \quad C = 539.44\,PF$$

we know that $h_{fe} \geq 4K + 2 + \frac{29}{K}$

$$\Rightarrow h_{fe} \geq 4(2.8169) + 2 + \frac{29}{2.8169}$$

$$\therefore h_{fe} \geq 44.5626$$

Advantages and disadvantages of RC Phase shift oscillator:

1) The circuit is simple to design.

2) It can produce the output over audio frequency range.

3) It produces sinusoidal output waveform.

The drawbacks of RC phase shift oscillator are

1) To change the frequency of oscillation in an RC phase shift oscillator, all the three capacitors or resistors should be changed simultaneously.

2) It is difficult to control the amplitude of the output signal, without affecting the frequency of oscillation.

3) Frequency stability is poor.

Problem: Find the capacitor C and h_{fe} for the transistor to provide a transistor to provide the frequency of oscillation of 10KHz of a transistorized oscillator designed with RC phase shift. Assume $R_1 = 25k\Omega$ $R_2 = 60K\Omega$, $R_c = 40K\Omega$, $R = 7.1K\Omega$ and $h_{ie} = 1.8K\Omega$.

Sol) Given $f_o = 10KHz$, $R_1 = 25K\Omega$, $R_2 = 60K\Omega$, $R_c = 40K\Omega$, $R = 7.1K\Omega$ and $h_{ie} = 1.8K\Omega$.

Frequency of oscillation $f_o = \frac{1}{2\pi RC\sqrt{6+4K}}$

$$\Rightarrow C = \frac{1}{2\pi f_o R\sqrt{6+4K}} = \frac{1}{2\pi f_o R\sqrt{6+4\frac{R_c}{R}}}$$

$$\Rightarrow C = \frac{1}{2\pi\times10\times10^{3}\times7.1\times10^{3}\sqrt{6+4\left(\frac{40}{7.1\times10^{3}}\right)}}$$

$$C = 0.41nF$$

we know that $h_{fe} \geq 4K + 23 + \frac{29}{K}$

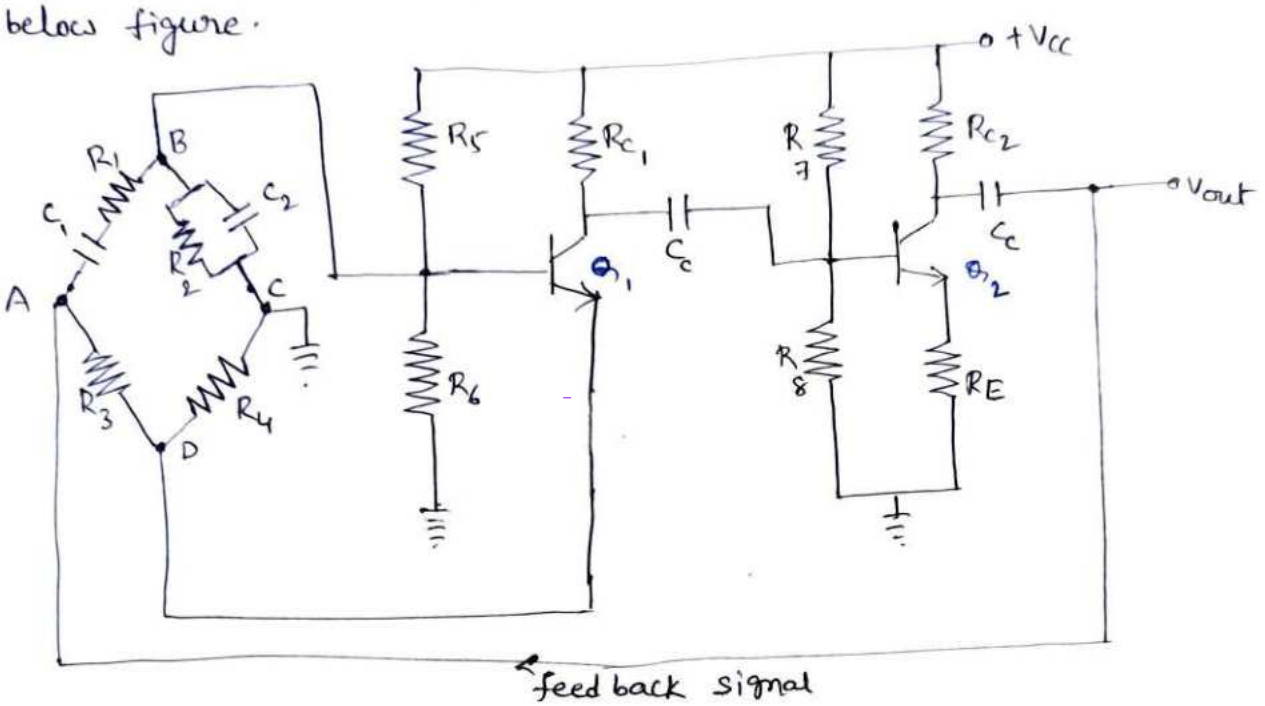
$$\Rightarrow h_{fe} \geq 4\left(\frac{R_c}{R}\right) + 23 + \frac{29}{(R_c/R)}$$

$$\Rightarrow h_{fe} \geq 4\left(\frac{40\times10^3}{7.1\times10^3}\right) + 23 + \frac{29\times7.1\times10^3}{40\times10^3}$$

$$\therefore h_{fe} \geq 50.67$$

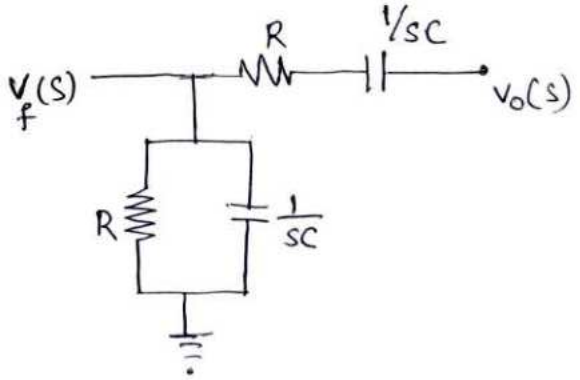
Wien-Bridge oscillator:

The circuit diagram for a wien-bridge oscillator is as shown in below figure.



fig(a): Wien-Bridge oscillator circuit

A wien-bridge oscillator circuit contains a two stage RC coupled amplifier which provides a phase shift of 360° (or) 0°.



fig(b): Equivalent Circuit

A balanced bridge is used as a feedback network in which there is no necessity for any additional phase shift.

The feedback network consists of a lead-lag network R_1-C_1 and R_2-C_2 and a potential divider R_3-R_4. The lead-lag network provides a positive feedback to the input of the first stage transistor Q_1 i.e base

of the transistor Q_1 and the voltage divider provides a negative feedback to the emitter of Q_1.

The frequency of oscillations is determined by the series element R_1, C_1 and parallel elements R_2, C_2 of the bridge and it is given as $f_0 = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}$

If $R_1 = R_2 = R$ and $C_1 = C_2 = C$ then $f_0 = \frac{1}{2\pi\sqrt{R^2C^2}}$

$$\therefore f_0 = \frac{1}{2\pi RC}$$

The bridge is said to be balanced if $\frac{R_3}{R_4} = \frac{R_1 + \frac{1}{j\omega C_1}}{R_2 \| \frac{1}{j\omega C_2}} = \frac{R_1 - \frac{j}{\omega C_1}}{R_2 \| \frac{-j}{\omega C_2}}$

$$\Rightarrow \frac{R_3}{R_4} = \frac{R_1 - \frac{j}{\omega C_1}}{\left(\frac{-jR_2}{\omega C_2}\right) \Big/ R_2 - \frac{j}{\omega C_2}}$$

$$\Rightarrow \frac{R_3}{R_4} = \frac{j\omega C_2}{R_2}\left(R_1 - \frac{j}{\omega C_1}\right)\left(R_2 - \frac{j}{\omega C_2}\right)$$

$$\Rightarrow \frac{R_3}{R_4} = \frac{j\omega C_2}{R_2}\left[R_1 R_2 - \frac{1}{\omega^2 C_1 C_2} - \frac{jR_2}{\omega C_1} - j\frac{R_1}{\omega C_2}\right]$$

$$\Rightarrow \frac{R_3}{R_4} = \frac{j\omega C_2}{R_2}\left[\left[R_1 R_2 - \frac{1}{\omega^2 C_1 C_2}\right] - \frac{j}{\omega}\left[\frac{R_2}{C_1} + \frac{R_1}{C_2}\right]\right]$$

$$\Rightarrow \frac{R_3}{R_4} = \frac{j\omega C_2}{R_2}\left[R_1 R_2 - \frac{1}{\omega^2 C_1 C_2}\right] + \frac{C_2}{R_2}\left[\frac{R_2}{C_1} + \frac{R_1}{C_2}\right]$$

Comparing imaginary parts on both sides we get

$$\frac{\omega C_2}{R_2}\left(R_1 R_2 - \frac{1}{\omega^2 C_1 C_2}\right) = 0 \Rightarrow R_1 R_2 - \frac{1}{\omega^2 C_1 C_2} = 0$$

$$\Rightarrow \omega^2 = \frac{1}{R_1 R_2 C_1 C_2}$$

$$\Rightarrow \omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$\therefore f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \quad (\because \omega = 2\pi f_0)$$

If $R_1 = R_2 = R$, $C_1 = C_2 = C$ then

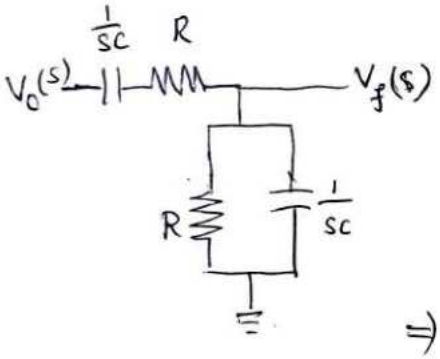
$$\boxed{f_0 = \frac{1}{2\pi RC}}$$

The ratio of R_3 and R_4 should be greater than 2 to provide a sufficient gain for the circuit to provide the desired frequency of oscillation.

Gain of the BJT amplifier used in Wien bridge oscillator

Assume $R_1 = R_2 = R$ and $C_1 = C_2 = C$. Then feed back circuit is as shown in figure (b).

From figure(b) $V_f(s) = V_0(s) \cdot \dfrac{\left(R \parallel \frac{1}{sC}\right)}{\left(R \parallel \frac{1}{sC}\right) + R + \frac{1}{sC}}$



$$\Rightarrow \frac{V_f(s)}{V_0(s)} = \frac{\left[\dfrac{R \cdot \frac{1}{sC}}{R + \frac{1}{sC}}\right]}{\dfrac{R \cdot \frac{1}{sC}}{R + \frac{1}{sC}} + R + \frac{1}{sC}}$$

$$\Rightarrow \frac{V_f(s)}{V_0(s)} = \frac{\dfrac{R}{RSC+1}}{\dfrac{R}{RSC+1} + R + \frac{1}{sC}} = \frac{\dfrac{R}{RSC+1}}{\dfrac{RSC + R^2S^2C^2 + RSC + RSC + 1}{(RSC+1)sC}}$$

$$\therefore \beta = \frac{V_f(s)}{V_0(s)} = \frac{RSC}{R^2S^2C^2 + 3RSC + 1}$$

We know that $A\beta = 1 \Rightarrow A = \dfrac{1}{\beta} = \dfrac{R^2S^2C^2 + 3RSC + 1}{RSC}$

$$\Rightarrow A = RSC + 3 + \frac{1}{RSC}$$

Substituting $S = j\omega = \dfrac{j}{RC}$

$$\Rightarrow A = R\left(\frac{j}{RC}\right)C + 3 + \frac{1}{R\left(\frac{j}{RC}\right)C}$$

$$A = j + 3 + \frac{1}{j} \Rightarrow \boxed{A = 3}$$

Therefore the gain of the BJT amplifier is atleast equal to 3 for oscillations to be occured in a wienbridge oscillator.

i.e $\boxed{A \geq 3}$

Problem: In a wien bridge oscillator if the value of R is 100KΩ, frequency of oscillation is 10KHz find the value of capacitor C.

Sol) For wien bridge oscillator the frequency of oscillation is

$$f_0 = \frac{1}{2\pi RC} \Rightarrow C = \frac{1}{2\pi R f_0} = \frac{1}{2\pi (100\times10^3)(10\times10^3)}$$

$$\therefore \quad C = 159PF.$$

UNIT III
LARGE SIGNAL AMPLIFIERS
(POWER AMPLIFIERS)

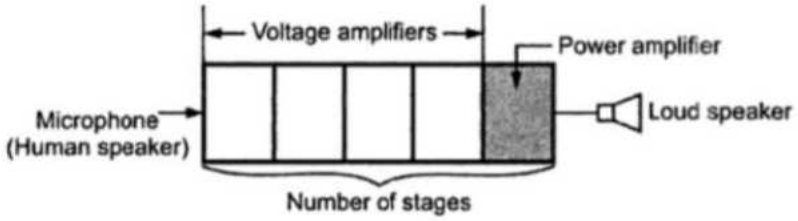
POWER AMPLIFIERS:

5.1 Concept of Large Signal Amplification

Consider a public address system (P.A.) or amplifying system as shown in the Fig. 5.1.

▶ **Figure 5.1**

Amplifying or P. A. system



The system consists of many stages connected in cascade. Hence basically it is a multistage amplifier. The input is sound signal of a human speaker and the output is given to the loud speaker which is an amplified input signal. The input and the intermediate stages are small signal amplifiers. The sufficient voltage gain is obtained by all the intermediate stages. Hence these stages are called **voltage amplifiers.**

But the last stage gives an output to the load like a loud speaker. Hence the last stage must be capable of delivering an appreciable amount of a.c. power to the load. So it must be capable of handling large voltage or current swings or in other words large signals. The main aim is to develop sufficient power hence the voltage gain is not important, in the last stage. Such a stage, which develops and feeds sufficient power to the load like loudspeaker, servomotor, handling the large signals is called **Large Signal Amplifier** or **Power Amplifier.**

Power amplifiers find their applications in the public address systems, radio receivers, driving servomotor in industrial control systems, tape players, T.V. receivers, cathode ray tubes etc.

5.2 Features of Power Amplifiers

The various features of power amplifiers are,

1. A power amplifier is the last stage of multistage amplifier. The previous stages develop sufficient gain and the **input signal level or amplitude of a power amplifier is large** of the order of few volts.
2. The **output of power amplifier has large current and voltage swings.** As it handles large signals called power amplifiers.
3. **The h-parameter analysis** is applicable to the small signal amplifiers and hence **can not be used for the analysis of power amplifiers.** The analysis of power amplifiers is carried out graphically by drawing a load line on the output characteristics of the transistors used in it.

4. The power amplifiers i.e large signal amplifiers are used to feed the loads like loud speakers having low impedance. So for maximum power transfer the impedance matching is important. Hence **the power amplifiers must have low output impedance**. Hence common collecter or emitter follower circuit is very common in power amplifiers. The common emitter circuit with a step down transformer for impedance matching is also commonly used in power amplifiers.
5. The power amplifiers develop an a.c. power of the order of few watts. Similarly large power gets dissipated in the form of heat, at the junctions of the transistors used in the power amplifiers. **Hence the transistors used in the power amplifiers are of large size, having large power dissipation rating, called power transistors.** Such transistors have heat sinks. A heat sink is a metal cap having bigger surface area, press fit on the body of a transistor, to get more surface area, in order to dissipate the heat to the surroundings. In general, the power amplifiers have bulky components.
6. A faithful reproduction of the signal, after the conversion, is important. Due to nonlinear nature of the transistor characteristics, there exists a harmonic distortion in the signal. Ideally signal should not be distorted. **Hence the analysis of signal distortion in case of the power amplifiers is important.**
7. Many a times, the power amplifiers are used in public address systems and many audio circuits to supply large power to the loud speakers. **Hence power amplifiers are also called audioamplifiers or audio frequency (A.F.) power amplifiers.**

5.3 Classification of Large Signal Amplifiers

For an amplifier, a quiescent operating point (Q point) is fixed by selecting the proper d.c. biasing to the transistors used. The quiescent operating point is shown on the load line, which is plotted on the output characteristics of the transistor. The position of the quiescent point on the load line decides the class of operation of the power amplifier. The various classes of the power amplifiers are :

i) Class A ii) Class B iii) Class C and iv) Class AB

5.3.1 Class A Amplifiers

The power amplifier is said to be class A amplifier if the Q point and the input signal are selected such that the output signal is obtained for a full input cycle.

> **Key Point**: *For this class, position of the Q point is approximately at the midpoint of the load line.*

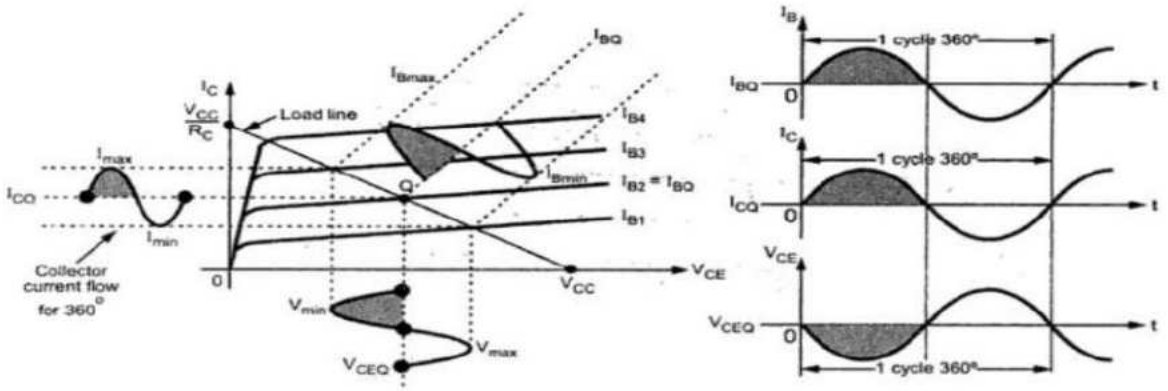
For all values of input signal, the transistor remains in the active region and never enters into cut-off or saturation region. When an a.c. input signal is applied, the collector voltage varies sinusoidally hence the collector current also varies sinusoidally. The collector current flows for 360° (full cycle) of the input signal. In other words, the angle of the collector current flow is 360° i.e. one full cycle.

The current and voltage waveforms for a class A operation are shown with the help of output characteristics and the load line, in the Fig. 5.6.

As shown in the Fig. 5.6, for full input cycle, a full output cycle is obtained. Here signal is faithfully reproduced, at the output, without any distortion. This is an important feature of a class A operation. The efficiency of class A operation is very small.

► **Figure 5.6**

Waveforms representing class A operation



5.3.2 Class B Amplifiers

The power amplifier is said to be class B amplifier if the Q point and the input signal are selected, such that the output signal is obtained only for one half cycle for a full input cycle.

> **Key Point**: *For this operation, the Q point is shifted on X-axis i.e. transistor is biased to cut-off.*

Due to the selection of Q point on the X-axis, the transistor remains, in the active region, only for positive half cycle of the input signal. Hence this half cycle is reproduced at the output. But in a negative half cycle of the input signal, the transistor enters into a cut-off region and no signal is produced at the output. The collector current flows only for 180° (half cycle) of the input signal. In other words, the angle of the collector current flow is 180° i.e. one half cycle.

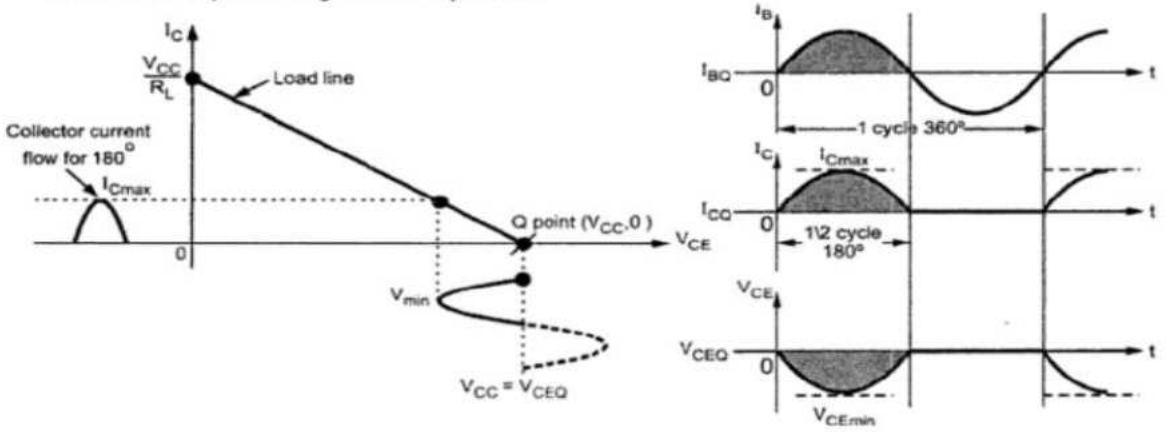
The current and voltage waveforms for a class B operation are shown in the Fig. 5.7.

As only a half cycle is obtained at the output, for full input cycle, the output signal is distorted in this mode of operation. To eliminate this distortion, practically two transistors are used in the alternate half cycles of the input signal. Thus overall a full cycle of output signal is obtained across the load. Each transistor conducts only for a half cycle of the input signal.

The efficiency of class B operation is much higher than the class A operation.

► **Figure 5.7**

Waveforms representing class B operation



5.3.3 Class C Amplifiers

The power amplifiers is said to be class C amplifier, if the Q point and the input signal are selected such that the output signal is obtained for less than a half cycle, for a full input cycle.

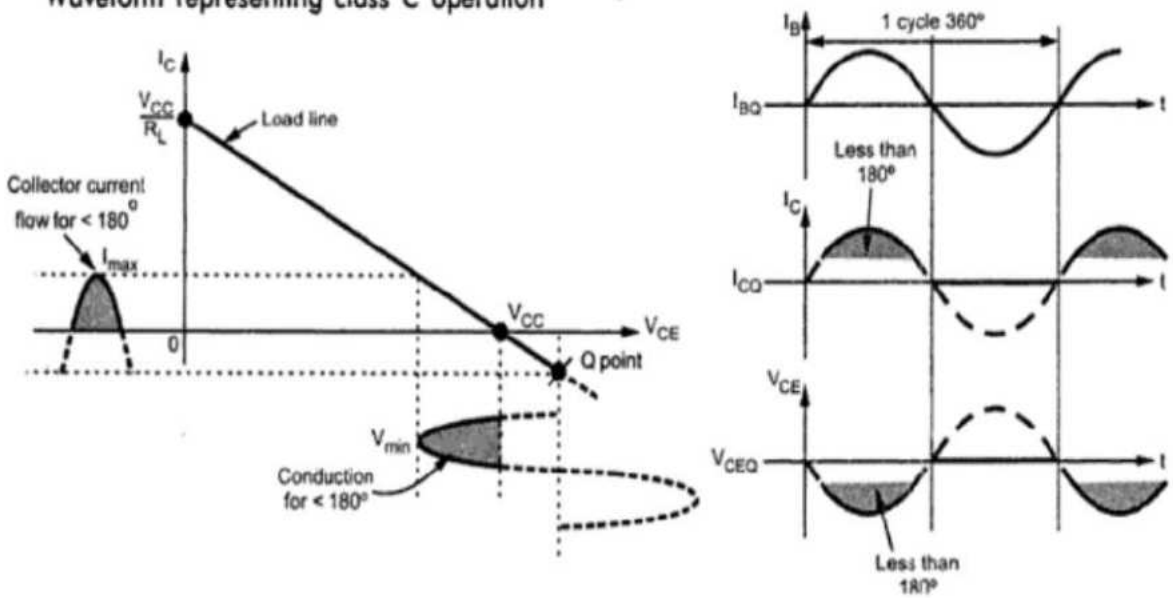
Key Point: *For this operation, the Q point is to be shifted below X-axis.*

Due to such a selection of the Q point, transistor remains active, for less than a half cycle. Hence only that much part is reproduced at the output. For remaining cycle of the input cycle, the transistor remains cut-off and no signal is produced at the output. The angle of the collector current flow is less than 180°.

The current and voltage waveforms for a class C amplifier operation are shown in the Fig. 5.8.

▶ **Figure 5.8**

Waveform representing class C operation



Key Point: *In class C operation, the transistor is biased well beyond cut-off. As the collector current flows for less than 180°, the output is much more distorted and hence the class C mode is never used for A.F. power amplifiers.*

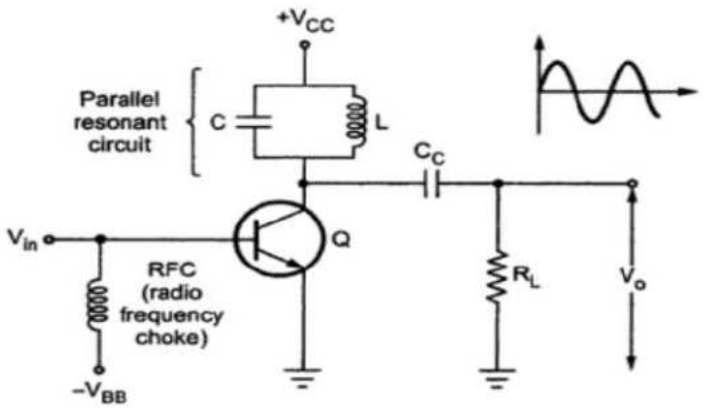
But the efficiency of this class of operation is much higher and can reach very close to 100%.

Applications : The class C operation is not suitable for audio frequency power amplifiers. The class C amplifiers are used in tuned circuits used in communication areas and in radio frequency (RF) circuits with tuned RLC loads. As used in tuned circuits, class C amplifiers are called **tuned amplifiers**. These are also used in mixer or converter circuits used in radio receivers and wireless communication systems.

The Fig. 5.9 shows the calss C tuned amplifier.

Figure 5.9

Class C tuned amplifier



The LC parallel circuit is a parallel resonant circuit. This circuit acts as a load impedance. Due to class C operation, the collector current consists of a series of pulses containing harmonics i.e. many other frequency components alongwith the fundamental frequency component of input. The parallel tuned circuit is designed to be tuned to the fundamental input frequency. Hence it elliminates the harmonics and produce a sine wave of fundamental component of input signal. As the transistor and coil losses are small, the most of the d.c. input power is converted to a.c. load power. Hence efficiency of class C is very high.

5.3.4 Class AB Amplifiers

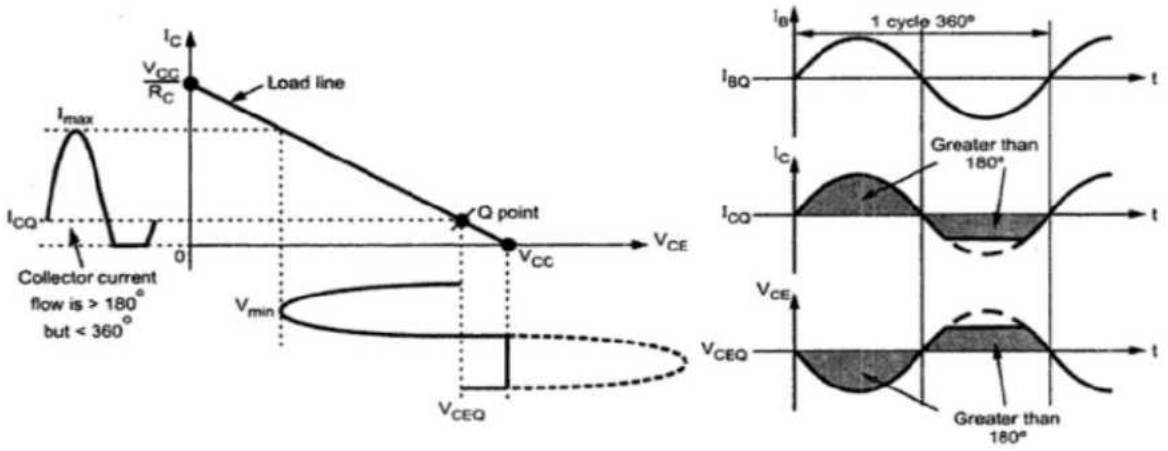
The power amplifier is said to be class AB amplifier, if the Q point and the input signal are selected such that the output signal is obtained for more than 180° but less than 360°, for a full input cycle.

Key Point: *The Q point position is above X-axis but below the midpoint of a load line.*

The current and voltage waveforms for a class AB operation, are shown in the Fig. 5.10.

Figure 5.10

Waveforms representing class AB operation



The output signal is distorted in class AB operation. The efficiency is more than class A but less than class B operation. The class AB operation is important to eliminate cross over distortion.

In general as the Q point moves away from the centre of the load line below towards the X-axis, the efficiency of class of operation increases.

5.5 Comparison of Amplifier Classes

The comparison of various amplifier classes is summarized in Table 5.1.

▶ **Table 5.1**

Class	A	B	C	AB
Operating Cycle	360°	180°	Less than 180°	180° to 360°
Position of Q point	Centre of load line	On X axis	Below X axis	Above X-axis but below the centre of load line
Efficiency	Poor, 25% to 50%	Better, 78.5%	High	Higher than A but less than B 50% to 78.5%
Distrotion	Absent No distortion	Present More than class A	Highest	Present

Key Point: *It is important to note that class C operation is never used for audio frequency amplifiers.*

This class is used in special areas of tuned circuits, such as radio or communications.

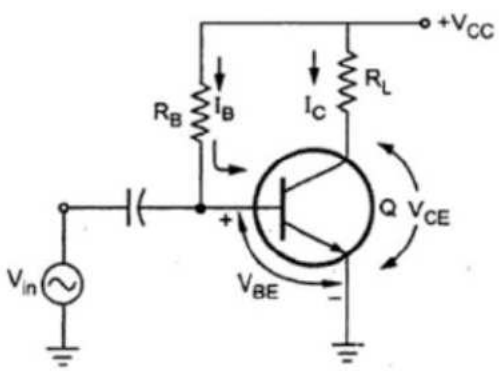
5.6 Analysis of Class A Amplifiers

The class A amplifiers are further classified as **directly coupled** and **transformer coupled** amplifiers. In directly coupled type, the load is directly connected in the collector circuit. While in the transformer coupled type, the load is coupled to the collector using a transformer called an output transformer. Let us study in detail the various aspects of the two types of Class A amplifiers.

5.7 Series Fed, Directly Coupled Class A Amplifier

▶ **Figure 5.13**

Large signal class A amplifier



A simple fixed-bias circuit can be used as a large signal class A amplifier as shown in the Fig. 5.13.

The difference between small signal version of this circuit is that the signals handled by this large signal circuit are of the order of few volts. Similarly the transistor used, is a power transistor. The value of R_B is selected in such a way that the Q point lies at the centre of the d.c. load line.

The circuit represents the directly coupled class A amplifier as the load resistance is directly connected in the collector circuit. Most of the times the load is a loudspeaker, the

impedance of which varies from 3 to 4 ohms to 16 ohms. The beta of the transistor used is less than 100.

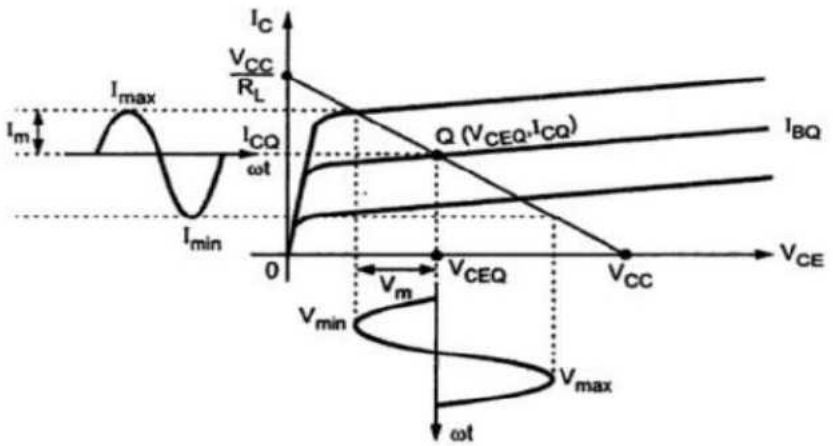
Key Point: *This is called **directly coupled**, as the load R_L is directly connected in the collector circuit of power transistor.*

The overall circuit handles large power, in the range of a few to tens of watts without providing much voltage gain.

The graphical representation of a class A amplifier is shown in the Fig. 5.14.

Figure 5.14

Graphical representation of class A amplifier



Applying Kirchhoff's voltage law to the circuit shown in the Fig. 5.13, we get

$$V_{CC} = I_C R_L + V_{CE}$$

$$\therefore \quad I_C R_L = -V_{CE} + V_{CC}$$

$$\therefore \quad I_C = \left[-\frac{1}{R_L}\right] V_{CE} + \frac{V_{CC}}{R_L} \qquad \ldots (1)$$

The equation is similar to equation (1) of section 7.3 and thus the slope of the load line is $-\frac{1}{R_L}$ while the Y-intercept is $\frac{V_{CC}}{R_L}$.

The change is because the collector resistance R_C is named as load resistance R_L in this circuit. The Q point is adjusted approximately at the centre of the load line.

5.7.1 D.C.Operation

The collector supply voltage V_{CC} and resistance R_B decides the d.c. base-bias current I_{BQ}. The expression is obtained applying KVL to the B-E loop and with $V_{BE} = 0.7$ V.

$$\therefore I_{BQ} = \frac{V_{CC} - 0.7}{R_B} \qquad \ldots (2)$$

The corresponding collector current is then,

$$I_{CQ} = \beta I_{BQ} \qquad \ldots (3)$$

From the equation (1), the corresponding collector to emitter voltage is,

$$V_{CEQ} = V_{CC} - I_{CQ} R_L \qquad \ldots (4)$$

Hence the Q point can be defined as Q (V_{CEQ}, I_{CQ}).

5.7.2 D.C.Power Input

The d.c. power input is provided by the supply. With no a.c input signal, the d.c. current drawn is the collector bias current I_{CQ} . Hence d.c. power input is,

$$P_{DC} = V_{CC} \cdot I_{CQ} \quad \ldots (5)$$

It is important to note that even if a.c. input signal is applied, the average current drawn from the d.c. supply remains same. Hence equation (5) represents d.c. power input to the class A series fed amplifier.

5.7.3 A.C. Operation

When an input a.c. signal is applied, the base current varies sinusoidally.

Assuming that the nonlinear distortion is absent, the nature of the collector current and collector to emitter voltage also vary sinusoidally as shown graphically in the Fig. 5.14.

The output current i.e. collector current varies around its quiescent value while the output voltage i.e collector to emitter voltage varies around its quiescent value. The varying output voltage and output current deliver an a.c. power to the load. Let us find the expressions for the a.c. power delivered to the load.

5.7.4 A.C.Power Output

For an alternating output voltage and output current swings, shown in the Fig. 5.14, we can write,

V_{min} = Minimum instantaneous value of the collector (output) voltage

V_{max} = Maximum instantaneous value of the collector (output) voltage

and V_{pp} = Peak to peak value of a.c. output voltage across the load.

$$\therefore V_{pp} = V_{max} - V_{min} \quad \ldots (6)$$

Now V_m = Amplitude (peak) of a.c. output voltage as shown in the Fig. 5.14.

$$\therefore V_m = \frac{V_{pp}}{2} = \frac{V_{max} - V_{min}}{2} \quad \ldots (7)$$

Similarly we can write for the output current as,

I_{min} = Minimum instantaneous value of the collector (output) current

I_{max} = Maximum instantaneous value of the collector (output) current

and I_{pp} = Peak to peak value of a.c. output (load) current

$$\therefore I_{pp} = I_{max} - I_{min} \quad \ldots (8)$$

Now I_m = Amplitude (peak) of a.c. output (load) current as shown in the Fig. 5.14

$$\therefore I_m = \frac{I_{pp}}{2} = \frac{I_{max} - I_{min}}{2} \quad \ldots (9)$$

Hence the r.m.s. values of alternating output voltage and current can be obtained as,

$$V_{rms} = \frac{V_m}{\sqrt{2}} \quad \ldots (10)$$

$$I_{rms} = \frac{I_m}{\sqrt{2}} \quad \ldots (11)$$

Hence we can write,

$$V_{rms} = I_{rms} R_L \quad \ldots (12)$$

i.e. $$V_m = I_m R_L \quad \ldots (13)$$

The a.c. power delivered by the amplifier to the load can be expressed by using r.m.s values, maximum i.e. peak values and peak to peak values of output voltage and current.

i) Using r.m.s values

$$\boxed{P_{ac} = V_{rms} I_{rms}} \quad \ldots (14)$$

or $$\boxed{P_{ac} = I_{rms}^2 R_L} \quad \ldots (15)$$

or $$\boxed{P_{ac} = \frac{V_{rms}^2}{R_L}} \quad \ldots (16)$$

ii) Using peak values

$$P_{ac} = V_{rms} I_{rms} = \frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}}$$

$\therefore$ $$\boxed{P_{ac} = \frac{V_m I_m}{2}} \quad \ldots (17)$$

or $$\boxed{P_{ac} = \frac{I_m^2 R_L}{2}} \quad \ldots (18)$$

or $$\boxed{P_{ac} = \frac{V_m^2}{2R_L}} \quad \ldots (19)$$

iii) Using peak to peak values

$$P_{ac} = \frac{V_m I_m}{2} = \frac{\left(\frac{V_{PP}}{2}\right)\left(\frac{I_{PP}}{2}\right)}{2}$$

$$\boxed{P_{ac} = \frac{V_{pp} I_{pp}}{8}} \quad \ldots (20)$$

or $$\boxed{P_{ac} = \frac{I_{pp}^2 R_L}{8}} \quad \ldots (21)$$

or $$\boxed{P_{ac} = \frac{V_{PP}^2}{8R_L}} \quad \ldots (22)$$

But as $V_{pp} = V_{max} - V_{min}$ and $I_{pp} = I_{max} - I_{min}$; from equation (20), the a.c. power can be expressed as below, for graphical calculations.

$$\boxed{P_{ac} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8}} \quad \ldots (22)$$

5.7.5 Efficiency

The efficiency of an amplifier represents the amount of a.c. power delivered or transferred to the load, from the d.c. source i.e. accepting the d.c. power input. The generalised expression for an efficiency of an amplifier is,

$$\% \eta = \frac{P_{ac}}{P_{dc}} \times 100 \quad \ldots (24)$$

Now for class A operation, we have derived the expressions for P_{ac} and P_{dc}, hence using equations (5) and (23), we can write

$$\% \eta = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8 V_{CC} I_{CQ}} \times 100 \quad \ldots (25)$$

The efficiency is also called **conversion efficiency** of an amplifier.

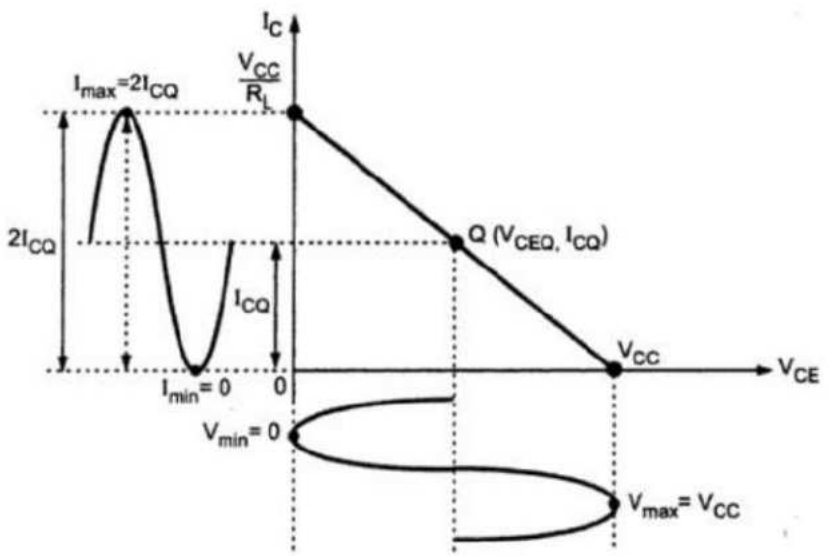
5.7.6 Maximum Efficiency

For maximum efficiency calculation, assume maximum swings of both the output voltage and the output current. The maximum swings are shown in the Fig. 5.15.

From the Fig. 5.15, we can see that the minimum voltage possible is zero and maximum voltage possible is V_{CC}, for a maximum swing. Similarly the minimum current is zero and the maximum current possible is $2\ I_{CQ}$, for a maximum swing.

Figure 5.15

Maximum voltage and current swings



$$\left.\begin{aligned} V_{max} &= V_{CC} \text{ and } V_{min} = 0 \\ I_{max} &= 2 I_{CQ} \text{ and } I_{min} = 0 \end{aligned}\right\} \text{ for maximum swing}$$

Using equation (25) we can write,

$$\% \eta_{max} = \frac{(V_{CC} - 0)(2I_{CQ} - 0)}{8 V_{CC} I_{CQ}} \times 100 = \frac{2 V_{CC} I_{CQ}}{8 V_{CC} I_{CQ}} \times 100$$

$$= 25\%$$

Key Point: *Thus* ***the maximum efficiency possible in case of directly coupled series fed class A amplifier is just 25%.***

This maximum efficiency is an ideal value. For a practical circuit, it is much less than 25%, of the order of 10 to 15%.

Key Point: ***Very low efficiency is the biggest disadvantage of class A amplifier.***

5.7.7 Power Dissipation

As stated earlier, power dissipation in large signal amplifier is also large. The amount of power that must be dissipated by the transistor is the difference between the d.c. power input P_{dc} and the a.c. power delivered to the load P_{ac}.

P_d = Power dissipation

i.e. $$\boxed{P_d = P_{DC} - P_{ac}} \quad \ldots (26)$$

The maximum power dissipation occurs when there is zero a.c. input signal. When a.c. input is zero, the a.c. power output is also zero. But transistor operates at quiescent condition, drawing d.c. input power from the supply equal to V_{CC} I_{CQ}. This entire power gets dissipated in the form of heat. Thus d.c. power input without a.c. input signal is the maximum power dissipation.

$$\boxed{(P_d)max = V_{CC} I_{CQ}} \quad \ldots (27)$$

Key Point: *Thus value of maximum power dissipation decides the maximum power dissipation rating of the transistor to be selected for the amplifier.*

5.7.8 Advantages and Disadvantages

The **advantages** of directly coupled class A amplifier can be stated as,

1. The circuit is simple to design and to implement
2. The load is connected directly in the collector circuit hence the output transformer is not necessary. This makes the circuit cheaper.
3. Less number of components required as load is directly coupled.

The disadvantages are :

1. The load resistance is directly connected in collector and carries the quiescent collector current. This causes considerable wastage of power.
2. Power dissipation is more. Hence power dissipation arrangements like heat sink are essential.
3. The output impedance is high hence circuit cannot be used for low impedance loads, such as loudspeakers.
4. The efficiency is very poor, due to large power dissipation.

Example 5.1 : *A series fed class A amplifier shown in Fig. 5.16, operates from D.C. source and applied sinusoidal input signal generates peak base current 9 mA. Calculate :*

i) Quiescent current I_{CQ}

ii) Quiescent voltage V_{CEQ}

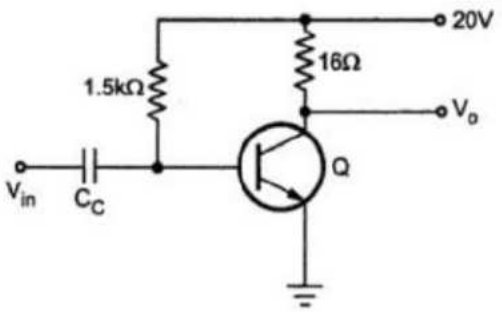
iii) D.C. input power P_{DC}

iv) A.C. output power P_{ac}

v) Efficiency.

Assume $\beta = 50$ and $V_{BE} = 0.7$ V.

Figure 5.16



Solution :

i) I_{CQ} $\quad I_{BQ} = \dfrac{V_{CC} - V_{BE}}{R_B} = \dfrac{20 - 0.7}{1.5 \times 10^3} = 12.87$ mA

$\quad I_{CQ} = \beta \times I_{BQ} = 50 \times 12.87 = 643.50$ mA

ii) V_{CEQ} $\quad V_{CC} = I_{CQ}R_L + V_{CEQ}$

$\therefore V_{CEQ} = V_{CC} - I_{CQ}R_L = 20 - 643.50 \times 10^{-3} \times 16 = 9.70$ volts

iii) P_{DC} $\quad P_{DC} = V_{CC} \times I_{CQ} = 20 \times 643.5 \times 10^{-3} = 12.87$ watt

iv) P_{ac} Peak current $i_b = 9$ mA

$\quad i_c = \beta i_b = 50 \times 9 = 450$ mA (peak)

$\therefore \quad i_{c(rms)} = \dfrac{i_{c\,(peak)}}{\sqrt{2}} = \dfrac{450}{\sqrt{2}} = 318.19$ mA $= I_{rms}$

$\therefore P_{ac} = I_{rms}^2 R_L = (318.19 \times 10^{-3})^2 \times 16 = 1.619$ watt.

v) **Efficiency** $\quad \eta = \dfrac{P_{ac}}{P_{DC}} \times 100 = \dfrac{1.619}{12.87} \times 100 = 12.58\ \%$

Ans. : $I_{CQ} = 643.5$ mA, $V_{CEQ} = 9.7$ V, $P_{DC} = 12.87$ W, $P_{ac} = 1.619$ W, $\eta = 12.58\%$

5.8 Transformer Coupled Class A Amplifier

As stated earlier, for maximum power transfer to the load, the impedance matching is necessary. For loads like loudspeaker, having low impedance values, impedance matching is difficult using directly coupled amplifier circuit. This is because loudspeaker resistance is in the range of 3 to 4 ohms to 16 ohms while the output impedance of series fed directly coupled class A amplifier is very much high. This problem can be eliminated by using a transformer to deliver power to the load.

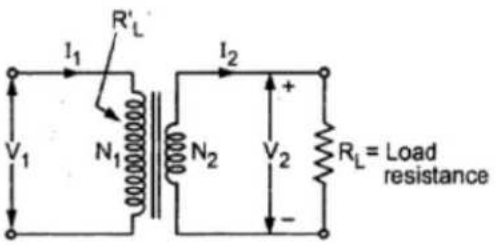
Key Point: *The transformer is called an* ***output transformer*** *and the amplifier is called* ***transformer coupled class A amplifier.***

Before studying the operation of the amplifier, let us revise few concepts regarding the transformer.

5.8.1 Properties of Transformer

▶ Figure 5.17

Transformer with load



Consider a transformer as shown in the Fig. 5.17 which is connected to a load of resistance R_L.

While analysing the transformer, it is assumed that the transformer is ideal and there are no losses in the transformer. Similarly the winding resistances are assumed to be zero.

Let N_1 = Number of turns on primary

N_2 = Number of turns on secondary

V_1 = Voltage applied to primary

V_2 = Voltage on secondary

I_2 = Primary current

i) Turns Ratio : The ratio of number of turns on secondary to the number of turns on primary is called turns ratio of the transformer denoted by n.

$$\therefore n = \text{Turns ratio} = \frac{N_2}{N_1} \quad \ldots (1)$$

Some times it is specified as $\frac{N_2}{N_1} : 1$ or $\frac{N_1}{N_2} : 1$.

ii) Voltage Transformation : The transformer transforms the voltage applied on one side to other side proportional to the turns ratio. The transformer can be step up or step down transformer.

$$\therefore \frac{V_2}{V_1} = \frac{N_2}{N_1} = n \quad \ldots (2)$$

In the amplifier analysis, the load impedance is going to be small. And the transformer is to be used for impedance matching. Hence it has to be a step down transformer. Hence

number of turns on primary are more than the secondary and turns ratio is less than unity, for such a step down transformer.

iii) Current Transformation : The current in the secondary winding is inversely proportional to the number of turns of the windings.

$$\therefore \frac{I_2}{I_1} = \frac{N_1}{N_2} = \frac{1}{n} \qquad \ldots (3)$$

iv) Impedance Transformation : As current and voltage get transformed from primary to secondary, an impedance 'seen' from either side (primary or secondary) also changes.

Now the impedance of the load on secondary is R_L as shown in the Fig. 5.17. The primary and secondary winding resistances are assumed to be zero. This load impedance R_L, gets reflected on the primary side and behaves as if connected in the primary side. Such impedance transferred from secondary to primary is denoted as R_L'.

Now using the equations (2) and (3) and the Fig. 5.17, we can write,

$$R_L = \frac{V_2}{I_2} \text{ and } R_L' = \frac{V_1}{I_1}$$

but $$V_1 = \frac{N_1}{N_2} V_2 \text{ and } I_1 = \frac{N_2}{N_1} I_2$$

$$\therefore R_L' = \frac{\frac{N_1}{N_2} V_2}{\frac{N_2}{N_1} I_2} = \left(\frac{N_1}{N_2}\right)^2 \times \frac{V_2}{I_2} = \frac{R_L}{\left(\frac{N_2}{N_1}\right)^2} = \frac{R_L}{n^2}$$

$$\therefore R_L' = \frac{R_L}{n^2} = \left(\frac{N_1}{N_2}\right)^2 R_L \qquad \ldots (4)$$

The R_L' is the **reflected impedance** and is related to the square of the turns ratio of the transformer. Remember that for a step down transformer, the secondary voltage is less than the primary. And high voltage side is always high impedance side. **Hence R_L' is always higher than R_L, for a stepdown transformer.**

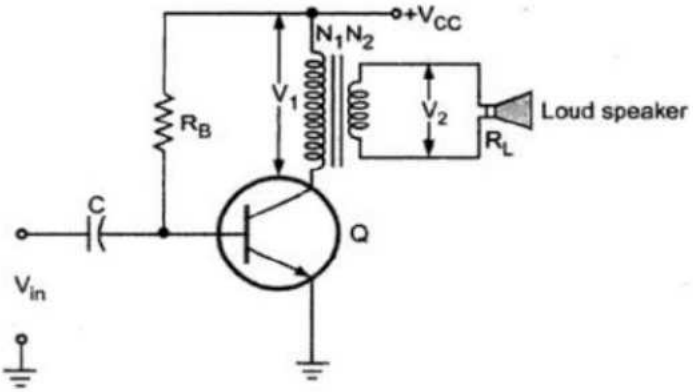
Key Point: *In the amplifier analysis, the load is on secondary while the active device, the transistor is on primary. Hence in all the calculations related to the transistor, the reflected load impedance R_L' must be considered rather than actual load impedance R_L.*

5.8.2 Circuit Diagram of Transformer Coupled Amplifier

The basic circuit of a transformer coupled amplifier is shown in the Fig. 5.18. The loudspeaker connected to the secondary acts as a load having impedance of R_L ohms.

► **Figure 5.18**

Transformer coupled class A amplifier



The transformer used is a step down transformer with the turns ratio as

$$n = N_2/N_1.$$

5.8.3 D.C. Operation

It is assumed that the winding resistances are zero ohms. Hence for d.c. purposes, the resistance is 0 Ω. There is no d.c. voltage drop across the primary winding of the transformer. The slope of the d.c. load line is reciprocal of the d.c. resistance in the collector circuit, which is zero in this case. Hence slope of the d.c. load line is ideally infinite. This tells that the d.c. load line in the ideal condition is a vertically straight line.

Applying Kirchhoff's voltage law to the collector circuit we get,

$$V_{CC} - V_{CE} = 0$$

i.e. $V_{CC} = V_{CE}$ ... drop across winding is zero

This is the d.c. bias voltage V_{CEQ} for the transistor.

So $$V_{CEQ} = V_{CC} \quad \text{... (5)}$$

Hence the d.c. load line is a vertical straight line passing through a voltage point on the X-axis which is $V_{CEQ} = V_{CC}$.

The intersection of d.c. load line and the base current set by the circuit is the quiescent operating point of the circuit. The corresponding collector current is I_{CQ}.

The d.c. load line is shown in the Fig. 5.19.

5.8.4 D.C Power Input

The d.c. power input is provided by the supply voltage with no signal input, the d.c. current drawn is the collector bias current I_{CQ}.

Hence the d.c. power input is given by,

So $$P_{DC} = V_{CC}\, I_{CQ} \quad \text{... (6)}$$

The expression is same as derived earlier for series fed directly coupled class A amplifier.

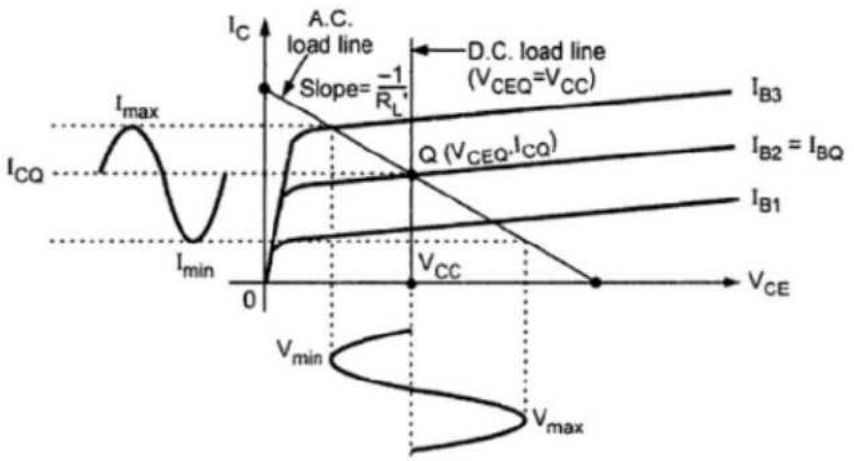
5.8.5 A.C. Operation

For the a.c. analysis, it is necessary to draw an a.c. load line on the output characteristics.

For a.c. purposes, the load on the secondary is the load impedance R_L ohms. And the reflected load on the primary i.e. R_L' can be calculated using the equation (4). The load line drawn with a slope of $\left(\frac{-1}{R_L'}\right)$ and passing through the operating point i.e. quiescent point Q is called **a.c. load line**. The d.c. and a.c. load lines are shown in the Fig. 5.19.

▶ Figure 5.19

Load lines for transformer coupled class A amplifier



The output current i.e. collector current varies around its quiescent value I_{CQ}, when a.c. input signal is applied to the amplifier. The corresponding output voltage also varies sinusoidally around its quiescent value V_{CEQ} which is V_{CC} in this case.

5.8.6 A.C. Output Power

The a.c. power developed is on the primary side of the transformer. While calculating this power, the primary values of voltage and current and reflected load R_L' must be considered. The a.c. power delivered to the load is on the secondary side of the transformer. While calculating load voltage, load current, load power the secondary voltage, current and the load R_L must be considered.

Let $V_{1\,m}$ = Magnitude or peak value of primary voltage

$V_{1\,rms}$ = R.M.S value of primary voltage

$I_{1\,m}$ = Peak value of primary current

$I_{1\,rms}$ = R.M.S value of primary current.

Hence the a.c. power developed on the primary is given by,

$$P_{ac} = V_{1\,rms}\, I_{1\,rms} \quad \ldots (7)$$

$$P_{ac} = I_{1\,rms}^2\, R_L' \quad \ldots (8)$$

$$P_{ac} = \frac{V_{1rms}^2}{R_L'} \quad \ldots (9)$$

$$P_{ac} = \frac{V_{1m}}{\sqrt{2}} \cdot \frac{I_{1m}}{\sqrt{2}} = \frac{V_{1m} I_{1m}}{2} \quad \ldots (10)$$

$$P_{ac} = \frac{I_{1m}^2 R_L'}{2} \quad \ldots (11)$$

$$P_{ac} = \frac{V_{1m}^2}{2 R_L'} \quad \ldots (12)$$

Similarly the a.c. power delivered to the load on secondary, also can be calculated, using secondary quantities.

Let V_{2m} = Magnitude or peak value of secondary or load voltage

$V_{2\,rms}$ = R.M.S value of secondary or load voltage

I_{2m} = Magnitude or peak value of secondary or load current.

I_{2rms} = R.M.S. value of secondary or load current

$$P_{ac} = V_{2rms}\ I_{2rms} = I_{2rms}^2\ R_L = \frac{V_{2rms}^2}{R_L} \quad \ldots (13)$$

or

$$P_{ac} = \frac{V_{2m}\ I_{2m}}{2} = \frac{I_{2m}^2 R_L}{2} = \frac{V_{2m}^2}{2R_L} \quad \ldots (14)$$

Power delivered on primary is same as power delivered to the load on secondary, assuming **ideal transformer**. Primary and Secondary values of voltages and currents are related to each other through the turns ratio of the transformer.

Key Point: *In practical circuit, the transformer can not be ideal. Hence the power delivered to the load on the secondary is slightly less than power developed on the primary. In such case, the transformer efficiency must be considered for calculating various parameters on the primary and secondary sides of the transformer.*

The slope of the a.c. load line can be expressed in terms of the primary current and the primary voltage.

The slope of the a.c. load line is,

$$= \frac{1}{R_L'} = \frac{I_{1m}}{V_{1m}} \quad \ldots (15)$$

The generalised expression for a.c. power output represented by the equation (24) in section (5.7), can be used as it is for transformer coupled amplifier. The expression is mentioned again for the convenience of the reader.

$$\therefore P_{ac} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8} \quad \ldots (16)$$

Key Point: *The a.c. power calculated is the power developed across the primary winding of the output transformer. Assuming ideal transformer, the power delivered to the load on secondary, is same as that developed across the primary. If the transformer efficiency is known, the power delivered to the load must be calculated from the power developed on the primary, considering the efficiency of the transformer.*

5.8.7 Efficiency

The general expression for the efficiency remains same as that given by equations (24) and (25) in section 5.7.

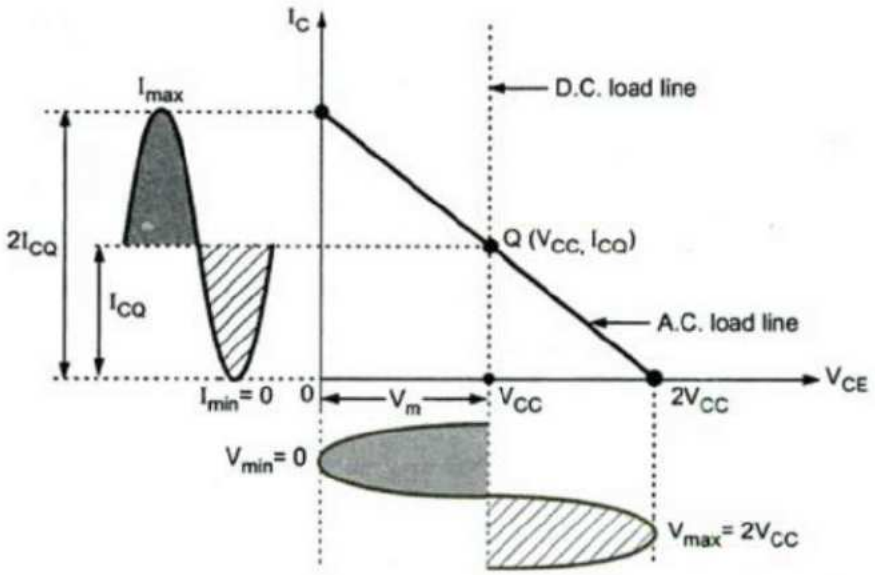
$$\% \eta = \frac{P_{ac}}{P_{dc}} \times 100 = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8 V_{CC} I_{CQ}} \times 100$$

5.8.8 Maximum Efficiency

Assume maximum swings of both the output voltage and output current, to calculate maximum efficiency, as shown in the Fig. 5.20.

▶ Figure 5.20

Maximum voltage and current swings



From the Fig. 5.20, assuming that the Q point is exactly at the centre of the load line, for maximum swing we can write,

$$\left.\begin{aligned} V_{min} &= 0 \text{ and } V_{max} = 2 V_{CC} \\ I_{min} &= 0 \text{ and } I_{max} = 2 I_{CQ} \end{aligned}\right\} \text{ for maximum swing}$$

Using equation (25) of section 5.7,

$$\% \eta_{max} = \frac{(2V_{CC} - 0)(2I_{CQ} - 0)}{8 V_{CC} I_{CQ}} \times 100$$

$$= \frac{4 V_{CC} I_{CQ}}{8 V_{CC} I_{CQ}} \times 100 = 50\%$$

Key Point: *Hence maximum possible theoretical efficiency in case of transformer coupled class A amplifier is 50%.*

For practical circuit it is about 30 to 35%, which is still much more than the directly coupled amplifier. For maximum efficiency, the power output is also maximum. For such maximum output power condition, it is seen that

$$V_{min} = 0 \text{ fand } V_{max} = 2\ V_{CC}$$

i.e. V_{1m} = peak value of primary voltage

$$= \frac{V_{max} - V_{min}}{2} = V_{CC}$$

$$\therefore V_{1m} = V_{CC} \text{ for maximum output power.}$$

Similarly from the maximum output current swing shown in the Fig. 5.20, we can say that the peak value of the output current is magnitude wise equal to the biasing collector current.

$$\therefore I_{1m} = I_{CQ} \text{ magnitude wise for maximum output power.}$$

Hence the equation (15) written for the magnitude of the slope of the a.c. load line can be modified as,

$$R'_L = \frac{V_{1m}}{I_{1m}} = \frac{V_{CC}}{I_{CQ}} \quad \text{... (15 a)}$$

Key Point: *This expression is applicable only in case of maximum power output condition.*

$$(P_{ac})\ max = \frac{1}{2} \frac{V_{CC}^2}{R'_L} \quad \text{... as } V_{1m} = V_{CC}$$

5.8.9 Power Dissipation

The power dissipation by the transistor is the difference between the a.c. power output and the d.c. power input. The power dissipated by the transformer is very small due to negligible (d.c.) winding resistances and can be neglected.

$$\therefore P_d = P_{DC} - P_{ac} \quad \text{... (16)}$$

When the input signal is larger, more power is delivered to the load and less is the power dissipation. But when there is no input signal, the entire d.c. input power gets dissipated in the form of heat, which is the maximum power dissipation.

$$\therefore (P_d)_{max} = V_{CC}\ I_{CQ} \quad \text{... (17)}$$

Thus the class A amplifier dissipates less power when delivers maximum power to the load. While it dissipates maximum power while delivering zero power to the load i.e. when load is removed and there is no a.c. input signal. The maximum power dissipation decides the maximum power dissipation rating for the power transistor to be selected for an amplifier.

5.8.10 Advantages and Disadvantages

The **advantages** of transformer coupled class A **amplifier** circuit are,

1. The efficiency of the operation is higher than directly coupled amplifier.
2. The d.c. bias current that flows through the load in case of directly coupled amplifier is stopped in case of transformer coupled.
3. The impedance matching required for maximum power transfer is possible.

The **disadvantages** are,

1. Due to the transformer, the circuit becomes bulkier, heavier and costlier compared to directly coupled circuit.
2. The circuit is complicated to design and implement compared to directly coupled circuit.
3. The frequency response of the circuit is poor.

Example 5.4 : *The loudspeaker of 8 Ω is connected to the secondary of the output transformer of a class A amplifier circuit. The quiescent collector current is 140 mA. The turns ratio of the transformer is 3:1. The collector supply voltage is 10V. If a.c. power delivered to the loudspeaker is 0.48 W, assuming ideal transformer, calculate :*

1. *A.C. power developed across primary*
2. *R.M.S. value of load voltage*
3. *R.M.S. value of primary voltage*
4. *R.M.S. value of load current*
5. *R.M.S. value of primary current*
6. *The D.C. power input*
7. *The efficiency*
8. *The power dissipation*

Solution : $R_L = 8\,\Omega$, $I_{CQ} = 140$ mA, $V_{CC} = 10$ V

$P_{ac} = 0.48$ W

The turns ratio are specified as $\frac{N_1}{N_2} : 1$ i.e. 3:1

$$\therefore \frac{N_1}{N_2} = 3$$

$$\therefore n = \frac{N_2}{N_1} = \frac{1}{3} = 0.3333$$

$$\therefore R'_L = \frac{R_L}{n^2}$$

$$= \frac{8}{(0.333)^2} = 72\,\Omega$$

1. As the transformer is ideal, whatever is the power delivered to the load, same is the power developed across primary.

$\therefore P_{ac}$ (across primary) = 0.48 W

2. Using equation (9),

$$\text{we get,} \quad P_{ac} = \frac{V_{1rms}^2}{R_L'}$$

$$\therefore 0.48 = \frac{V_{1rms}^2}{72}$$

$$V_{1rms}^2 = 34.56$$

$$\therefore V_{1rms} = 5.8787 \text{ V on primary.}$$

But r.m.s. value of the load voltage is V_{2rms}

$$\text{So} \quad \frac{(V_1)_{rms}}{(V_2)_{rms}} = \frac{N_1}{N_2} = \frac{3}{1}$$

$$\therefore (V_2)_{rms} = \frac{(V_1)_{rms}}{3} = \frac{5.8787}{3} = 1.9595 \text{ V}$$

This is the r.m.s. value of the load voltage.

3. The r.m.s value of the primary voltage is $(V_1)_{rms}$ as calculated above.

$$\therefore (V_1)_{rms} = 5.8787 \text{ V}$$

4. The power delivered to the load $= I_{2rms}^2 \times R_L$ ... refer eq. 13.

$$\therefore 0.48 = I_{2rms}^2 \times 8$$

$$\therefore I_{2rms}^2 = 0.06$$

$$\therefore I_{2\,rms} = 0.2449 \text{ A}$$

This is the r.m.s value of the load current as the resistance value used is R_L and not R_L'.

5. The r.m.s values of primary and secondary are related through the transformation ratio.

$$\therefore \frac{(I_1)_{rms}}{(I_2)_{rms}} = \frac{N_2}{N_1} = n = 0.333$$

$$\therefore (I_1)_{rms} = (I_2)_{rms} \times n = 0.2449 \times 0.333 = 0.0816\text{A} = 81.64 \text{ mA.}$$

6. The d.c. power input is,

$$P_{DC} = V_{CC}\, I_{CQ} = 10 \times 140 \times 10^{-3} = 1.4 \text{ W}$$

7. $$\% \eta = \frac{P_{ac}}{P_{dc}} \times 100 = \frac{0.48}{1.4} \times 100 = 34.28\%$$

8. $$P_d = P_{DC} - P_{ac} = 1.4 - 0.48 = 0.92 \text{ W}$$

This is the power dissipation. ■

5.10 Analysis of Class B Amplifiers

As stated earlier, for class B operation, the quiescent operating point is located on the X-axis itself. Due to this collector current flows only for a half cycle for a full cycle of the input signal. Hence the output signal is distorted. To get a full cycle across the load, a pair of transistors is used in class-B operation. The two transistors conduct in alternate half cycles of the input signal and a full cycle across the load is obtained. The two transistors are identical in characteristics and called matched transistors.

Depending upon the types of the two transistors whether p-n-p or n-p-n, the two circuit configurations of class B amplifier are possible. These are,

1. When both the transistors are of same type i.e. either n-p-n or p-n-p then the circuit is called **push-pull class B** A.F. power amplifier circuit.
2. When the two transistors form a complementary pair i.e. one n-p-n and other p-n-p then the circuit is called **complementary symmetry class B** A.F. power amplifier circuit. Let us analyse these two circuits of class B amplifiers in detail.

5.11 Push Pull Class B Amplifier

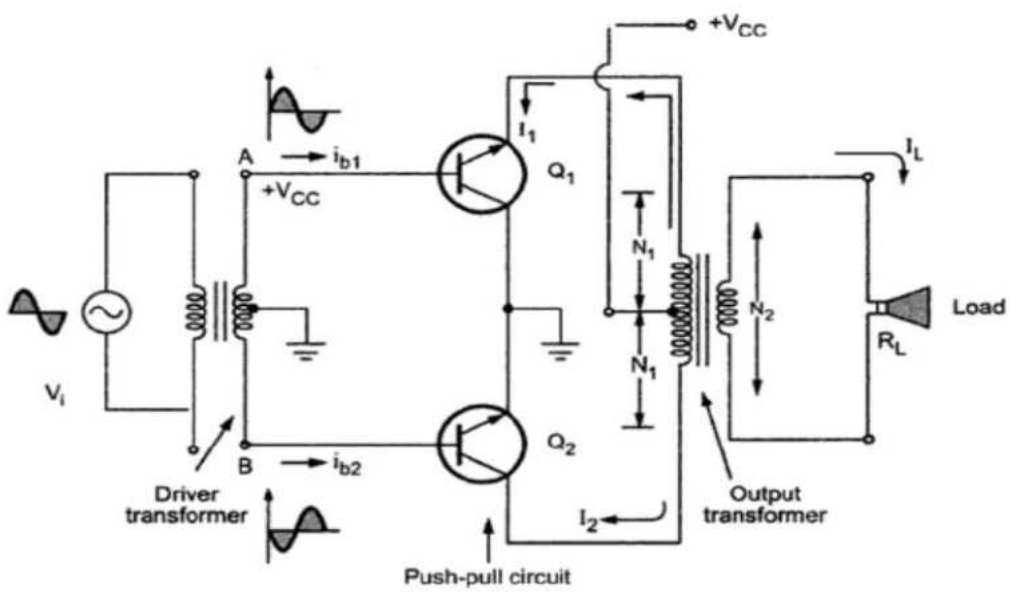
The push pull circuit requires two transformers, one as input transformer called **driver transformer** and the other to connect the load called **output transformer**. The input signal is applied to the primary of the driver transformer. Both the transformers are centre tapped transformers. The push pull class B amplifier circuit is shown in the Fig. 5.25.

In the circuit, both Q_1 and Q_2 transistors are of n-p-n type. The circuit can use both Q_1 and Q_2 of p-n-p type. In such a case, the only change is that the supply voltage must be $-V_{CC}$, the basic circuit remains the same. Generally the circuit using n-p-n transistors is used. Both the transistors are in common emitter configuration.

The driver transformer drives the circuit. The input signal is applied to the primary of the driver transformer. The centre tap on the secondary of the driver transformer is grounded. The centre tap on the primary of the output transformer is connected to the supply voltage + V_{CC}.

► **Figure 5.25**

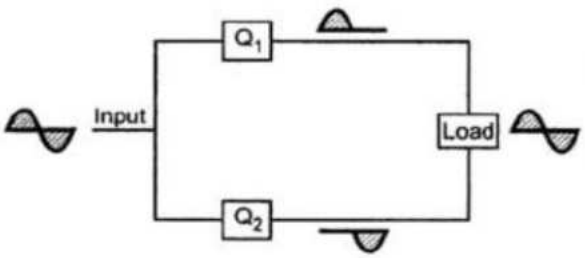
Push pull class B amplifier



With respect to the centre tap, for a positive half cycle of input signal, the point A shown on the secondary of the driver transformer will be positive. While the point B will be negative. Thus the voltages in the two halves of the secondary of the driver transformer will be equal but with opposite polarity. Hence the input signals applied to the base of the transistors Q_1 and Q_2 will be 180° out of phase.

▶ Figure 5.26

Basic push pull operation



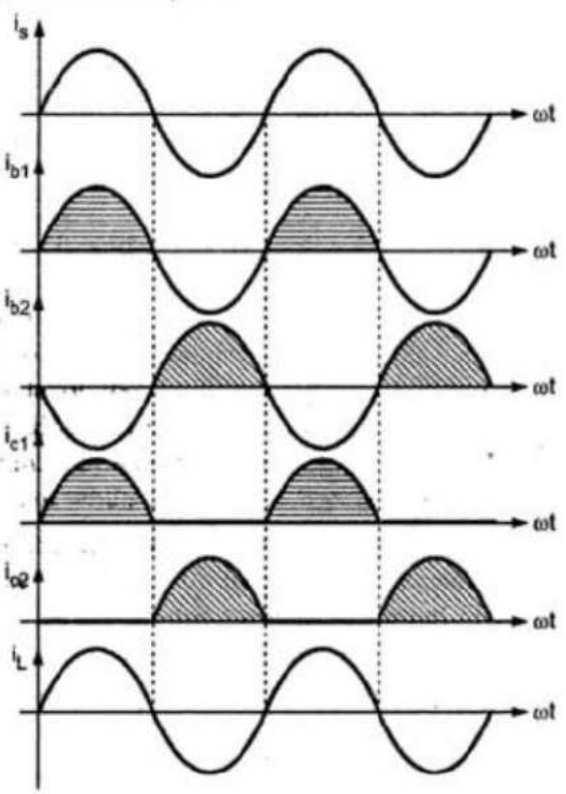
The transistor Q_1 conducts for the positive half cycle of the input producing positive half cycle across the load. While the transistor Q_2 conducts for the negative half cycle of the input producing negative half cycle across the load. Thus across the load, we get a full cycle for a full input cycle. The basic push pull operation is shown in the Fig. 5.26.

When point A is positive, the transistor Q_1 gets driven into an active region while the transistor Q_2 is in cut off region. While when point A is negative, the point B is positive, hence the transistor Q_2 gets driven into an active region while the transistor Q_1 is in cut off region.

The waveforms of the input current, base currents, collector currents and the load current are shown in the Fig. 5.27.

▶ Figure 5.27

Waveforms for push pull class B amplifier



Key Point: *For the output transformer, the number of the turns of each half of the primary is N_1 while the number of the turns on the secondary is N_2. Hence the total number of primary turns is $2N_1$. So turns ratio of the output transformer is specified as $2N_1$. So turns ratio of the output transformer is specified as $2N_1 : N_2$.*

5.11.1 D.C.Operation

The d.c. biasing point i.e. Q point is adjusted on the X-axis such that $V_{CEQ} = V_{CC}$ and I_{CEQ} is zero. Hence the co-ordinates of the Q point are (V_{CC}, 0). There is no d.c. base bias voltage.

5.11.2 D.C.Power Input

Each transistor output is in the form of half rectified waveform. Hence if I_m is the peak value of the output current of each transistor, the d.c. or average value is $\frac{I_m}{\pi}$, due to half rectified waveform. **The two currents, drawn by the two transistors, form the d.c. supply are in the same direction. Hence the total d.c. or average current drawn from the supply is the algebraic sum of the individual average current drawn by each transistor.**

$$\therefore \quad \boxed{I_{dc} = \frac{I_m}{\pi} + \frac{I_m}{\pi} = \frac{2\,I_m}{\pi}} \qquad \ldots (1)$$

The total d.c. power input is given by,

$$P_{DC} = V_{CC} \times I_{dc}$$

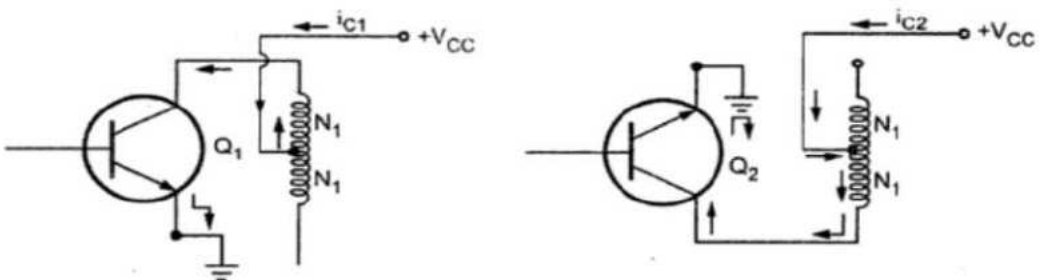
$$\therefore \quad \boxed{P_{DC} = \frac{2}{\pi} V_{CC}\ I_m} \qquad \ldots (2)$$

5.11.3 A.C.Operation

When the a.c. signal is applied to the driver transformer, for positive half cycle Q_1 conducts. The path of the current drawn by the Q_1 is shown in the Fig. 5.28.

For the negative half cycle Q_2 conducts. The path of the current drawn by the Q_2 is shown in the Fig. 5.28 (b).

Figure 5.28



(a) Q_1 conduction (b) Q_2 conduction

It can be seen that when Q_1 conducts, lower half of the primary of the output transformer does not carry any current. Hence only N_1 number of turns carry the current. While when Q_2 conducts, upper half of the primary does not carry any current. Hence again only N_1 number of turns carry the current. Hence the reflected load on the primary can be written as,

$$\therefore \quad \boxed{R'_L = \frac{R_L}{n^2}} \qquad \ldots (3)$$

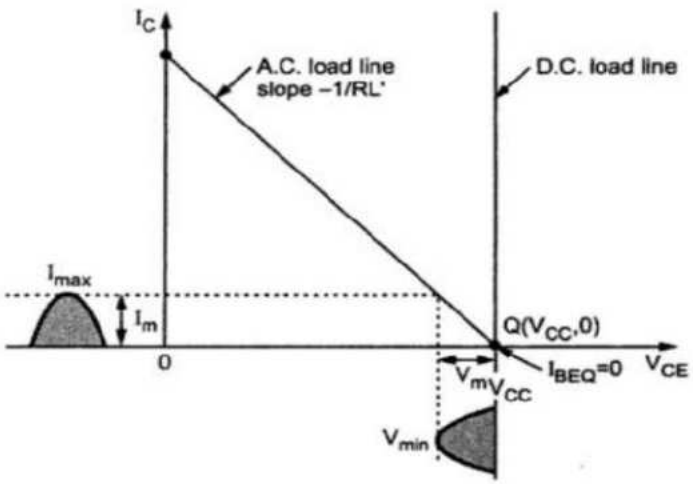
where $n = \frac{N_2}{N_1}$

It is important to note that the step down turns ratio is $2N_1 : N_2$ but while calculating the reflected load, the ratio n becomes N_2/N_1. So each transistor shares equal load which is the reflected load R'_L given by the equation (3).

The slope of the a.c. load line is $-1/R'_L$ while the d.c. load line is the vertical line passing through the operating point Q on the x-axis. The load lines are shown in the Fig. 5.29.

Figure 5.29

Load lines for push pull class B amplifier



The slope of the a.c. load line (magnitude of slope) can be represented in terms of V_m and I_m as,

$$\frac{1}{R'_L} = \frac{I_m}{V_m}$$

$$\therefore \quad \boxed{R'_L = \frac{V_m}{I_m}} \qquad \ldots (4)$$

where I_m = Peak value of the collector current

5.11.4 A.C. Power Output

As I_m and V_m are the peak values of the output current and the output voltage respectively, then

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

and $$I_{rms} = \frac{I_m}{\sqrt{2}}$$

Hence the a.c. power output is expressed as,

$$P_{ac} = V_{rms}\ I_{rms} = I^2_{rms}\ R'_L = \frac{V^2_{rms}}{R'_L} \qquad \ldots (5)$$

While using peak values it can be expressed as,

$$\therefore \boxed{P_{ac} = \frac{V_m I_m}{2} = \frac{I_m^2 R_L'}{2} = \frac{V_m^2}{2R_L'}} \quad \ldots (6)$$

5.11.5 Efficiency

The efficiency of the class B amplifier can be calculated using the basic equation.

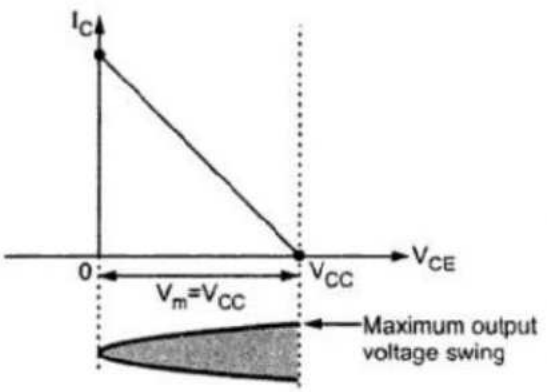
$$\%\eta = \frac{P_{ac}}{P_{DC}} \times 100 = \frac{\left(\frac{V_m I_m}{2}\right)}{\frac{2}{\pi} V_{CC} I_m} \times 100$$

$$\therefore \boxed{\%\eta = \frac{\pi}{4} \frac{V_m}{V_{CC}} \times 100} \quad \ldots (7)$$

5.11.6 Maximum Efficiency

From the equation (7), it is clear that as the peak value of the collector voltage V_m increases, the efficiency increases. The maximum value of V_m possible is equal to V_{CC} as shown in the Fig. 5.30.

Figure 5.30



$$\boxed{V_m = V_{CC} \text{ for maximum } \eta}$$

$$\therefore \%\,\eta_{max} = \frac{\pi}{4} \times \frac{V_{CC}}{V_{CC}} \times 100$$

$$= 78.5\ \%$$

Key Point: *Thus the maximum possible theoretical efficiency in case of push pull class B amplifier is 78.5% which is much higher than the transformer coupled class A amplifier.*

For practical circuits it is upto 65 to 70%.

Key Point: *Practically the collector-emitter voltage of transistor is neglected as small. But if* $V_{CE(min)}$ *is given then maximum collector voltage* V_m *reduces by* $V_{CE(min)}$ *and becomes* $V_m = V_{CC} - V_{CE(min)}$ *under maximum efficiency condition.*

5.11.7 Power Dissipation

The power dissipation by both the transistors is the difference between a.c. power output and d.c. power input.

$$\therefore P_d = P_{DC} - P_{ac} = \frac{2}{\pi} V_{CC} I_m - \frac{V_m I_m}{2}$$

$$\therefore P_d = \frac{2}{\pi} V_{CC} \frac{V_m}{R'_L} - \frac{V_m^2}{2R'_L} \quad \ldots (8)$$

Let us find out the condition for maximum power dissipation. In case of class A amplifier, it is maximum when no input signal is there. But in class B operation, when the input signal is zero, $V_m = 0$ hence the power dissipation is zero and not the maximum.

Maximum power dissipation : The condition for maximum power dissipation can be obtained by differentiating the equation (8) with respect to V_m and equating it to zero.

$$\therefore \frac{d P_d}{d V_m} = \frac{2}{\pi} \frac{V_{CC}}{R'_L} - \frac{2V_m}{2R'_L} = 0$$

$$\therefore \frac{2}{\pi} \frac{V_{CC}}{R'_L} = \frac{V_m}{R'_L}$$

$$\boxed{V_m = \frac{2}{\pi} V_{CC}} \quad \ldots \text{ For maximum power dissipation} \quad \ldots (9)$$

This is the **condition for maximum power dissipation**. Hence the maximum power dissipation is,

$$(P_d)_{max} = \frac{2}{\pi} V_{CC} \times \frac{2}{\pi} \frac{V_{CC}}{R'_L} - \frac{4}{\pi^2} \frac{V_{CC}^2}{2 R'_L}$$

$$= \frac{4}{\pi^2} \frac{V_{CC}^2}{R'_L} - \frac{2}{\pi^2} \frac{V_{CC}^2}{R'_L}$$

$$\therefore \boxed{(P_d)_{max} = \frac{2}{\pi^2} \frac{V_{CC}^2}{R'_L}} \quad \ldots (10)$$

Key Point: *For maximum efficiency, $V_m = V_{CC}$ hence the power dissipation is not maximum when the efficiency is maximum. And when power dissipation is maximum, efficiency is not maximum.* ***So maximum efficiency and maximum power dissipation do not occur simultaneously,*** *in case of class B amplifiers.*

Now $P_{ac} = \frac{V_m^2}{2 R'_L}$

and $V_m = V_{CC}$ is the maximum condition.

Hence $(P_{ac})_{max} = \frac{V_{CC}^2}{2 R'_L}$ ... (11)

Now $(P_d)_{max} = \frac{2V_{CC}^2}{\pi^2 R'_L} = \frac{4}{\pi^2}\left(\frac{V_{CC}^2}{2 R'_L}\right)$

$\therefore (P_d)_{max} = \frac{4}{\pi^2} (P_{ac})_{max}$ ... (12)

This much power is dissipated by both the transistors hence the maximum power dissipation per transistor is $(P_d)_{max} / 2$.

$$\therefore (P_d)_{max} \text{per transistor} = \frac{\frac{4}{\pi^2}(P_{ac})_{max}}{2}$$

$$\boxed{\therefore (P_d)_{max} \text{per transistor} = \frac{2}{\pi^2}(P_{ac})_{max}} \quad \ldots (13)$$

This is the **maximum power dissipation rating** of each transistor. For example, if 10 W maximum power is to be supplied to the load, then power dissipation rating of each transistor should be $\frac{2}{\pi^2} \times 10$ i.e. 2.02 W.

5.11.8 Harmonic Distortion

Let the base input currents are sinusoidal in nature and given by,

$$i_{b1} = I_{Bm} \cos \omega t \text{ and } i_{b2} = - I_{Bm} \cos \omega t$$

The negative sign indicates that both are 180° out of phase.

Due to nonlinear dynamic characteristics, the collector current of the two transistors can be expressed in terms of harmonic components as,

$$i_{c1} = I_{CQ} + B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t + B_3 \cos 3\omega t + \ldots \quad \ldots (14)$$

Now $i_{b1} = - I_{Bm} \cos \omega t = I_{Bm} \cos (\omega t + \pi)$

Hence the collector current for the second transistor can be obtained by replacing ωt by $\omega t + \pi$, in the expression for i_{c1}.

$$\therefore i_{c2} = I_{CQ} + B_0 + B_1 \cos(\omega t + \pi) + B_2 \cos 2(\omega t + \pi p) + \ldots$$

$$= I_{CQ} + B_0 - B_1 \cos \omega t + B_2 \cos 2\omega t - B_3 \cos 3\omega t + \ldots \quad \ldots (15)$$

Now the load current is the difference between the two. This is because, in the primary of the transformer the two currents are in opposite direction.

$$\therefore i_L = i_{c1} - i_{c2}$$

$$= (I_{CQ} + B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t + B_3 \cos 3\omega t + \ldots)$$

$$- (I_{CQ} + B_0 - B_1 \cos \omega t + B_2 \cos 2\omega t - B_3 \cos 3\omega t + \ldots)$$

$$\boxed{\therefore i_L = 2 B_1 \cos \omega t + 2 B_3 \cos 3\omega t + \ldots} \quad \ldots (16)$$

It can be seen that **the even harmonic components 2nd, 4th, 6th and so on, get eliminated. Similarly the d.c. component also gets eliminated.** Hence the total distortion is less and as d.c. component flowing is zero, there is no possibility of d.c. saturation of the core. Hence the percentage harmonic distortion is only due to odd harmonics given by,

$$\% D_3 = \frac{|B_3|}{|B_1|} \times 100 \text{ , } \% D_5 = \frac{|B_5|}{|B_1|} \times 100 \ \ldots$$

Hence the total harmonic distortion is,

$$\boxed{\% D = \sqrt{D_3^2 + D_5^2 + D_7^2 + \ldots} \times 100} \quad \ldots (17)$$

This is based on the assumption that the two transistors are exactly matched. Otherwise even harmonics may be present in the output signal.

5.11.9 Advantages and Disadvantages

The advantages of push pull class B operation are :

1. The efficiency is much higher than the class A operation.
2. When there is no input signal, the power dissipation is zero.
3. The even harmonics get cancelled. This reduces the harmonic distortion.
4. As the d.c. current components flow in opposite direction through the primary winding, there is no possibility of d.c. saturation of the core.
5. Ripples present in supply voltage also get eliminated.
6. Due to the transformer, impedance matching is possible.

The disadvantages of the circuit are :

1. Two center tap transformers are necessary.
2. The transformers, make the circuit bulky and hence costlier.
3. Frequency response is poor.

Example 5.9 *A class B, push pull amplifier drives a load of 16 Ω , connected to the secondary of the ideal transformer. The supply voltage is 25 V. If the number of turns on the primary is 200 and the number of turns on the secondary is 50, calculate maximum power output, d.c. power input, efficiency and maximum power dissipation per transistor.*

Solution : $R_L = 16\ \Omega$ $V_{CC} = 25$ V

Now $2N_1 = 200$ $N_2 = 50$

$\therefore N_1 = 100$

$\therefore n = \frac{N_2}{N_1} = \frac{50}{100} = 0.5$

$\therefore R'_L = \frac{R_L}{n^2} = \frac{16}{(0.5)^2}$

$= 64\ \Omega$

For maximum power output, $V_m = V_{CC}$

i) $(P_{ac})_{max} = \frac{1}{2}\frac{V_{CC}^2}{R'_L} = \frac{1}{2} \times \frac{(25)^2}{64}$

$= 4.8828$ W

ii) $P_{dc} = \frac{2}{\pi} V_{CC}\, I_m$

Now $\frac{V_m}{I_m} = R'_L$

and $V_m = V_{CC}$ ... refer equation (4)

$\therefore I_m = \frac{V_{CC}}{R'_L} = \frac{25}{64} = 0.3906$ A

$\therefore P_{DC} = \frac{2}{\pi} \times 25 \times 0.3906$

$= 6.2169$ W

iii) $\% \eta = \frac{P_{ac}}{P_{DC}} \times 100 = \frac{4.8828}{6.2169} \times 100$

$= 78.5\%$

iv) $(P_d)_{max} = \frac{2}{\pi^2} \times (P_{ac})_{max}$ for each transistor

$= \frac{2}{\pi^2} \times 4.8828$

$= 0.9894 \text{ W} = 1 \text{ W}$

5.12 Complementary Symmetry Class B Amplifier

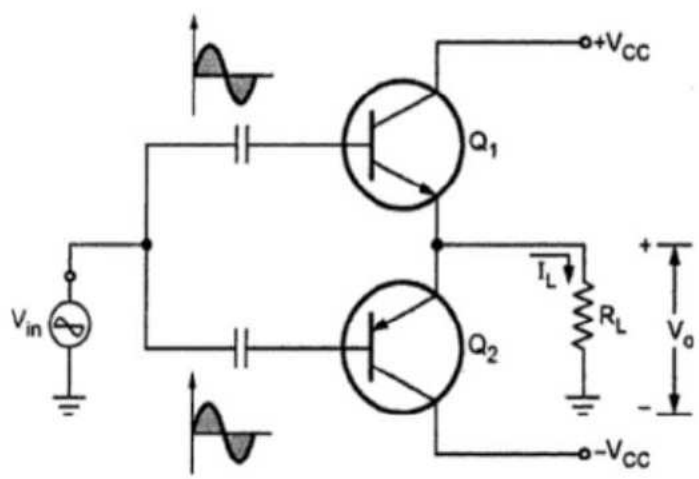
As stated earlier, instead of using same type of transistors (n-p-n or p-n-p), one n-p-n and other p-n-p is used, the amplifier circuit is called as complementary symmetry class B amplifier. This circuit is transformer less circuit. But with common emitter configuration, it becomes difficult to match the output impedance for maximum power transfer without an output transformers. Hence the matched pair of complementary transistors are used in common collector (emitter follower) configuration, in this circuit.

Key Point: *This is because common collector configuration has lowest output impedance and hence the impedance matching is possible.*

In addition, voltage feedback can be used to reduce the output impedance for matching.

▶ **Figure 5.32**

Complementary symmetry class B amplifier



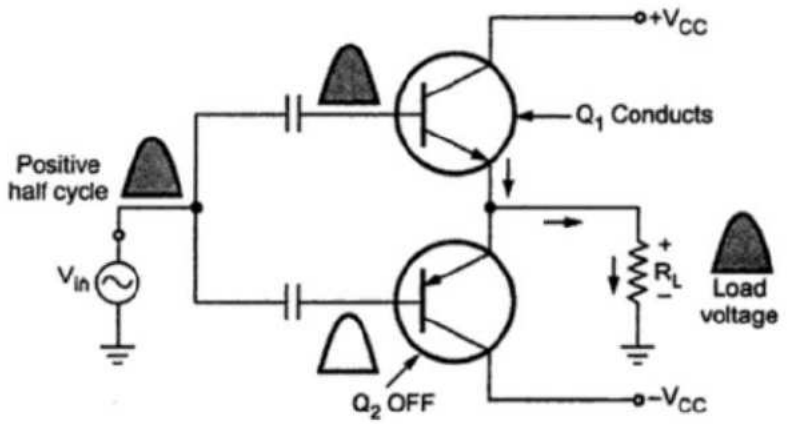
The basic circuit of complementary symmetry class-B amplifier is shown in the Fig. 5.32.

The circuit is driven from a dual supply of $\pm V_{CC}$. The transistor Q_1 is n-p-n while Q_2 is of p-n-p type.

In the positive half cycle of the input signal, the transistor Q_1 gets driven into active region and starts conducting. The same signal gets applied to the base of the Q_2 but as it is of complementary type, remains in off condition, during positive half cycle. This results into positive half cycle across the load R_L. This is shown in the Fig. 5.33.

▶ **Figure 5.33**

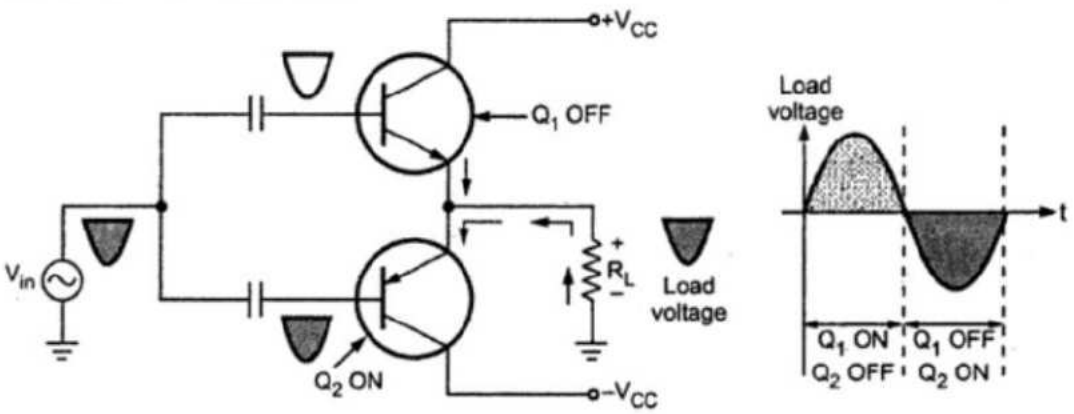
Positive half cycle operation



During the negative half cycle of the signal, the transistor Q_2 being p-n-p gets biased into conduction. While the transistor Q_1 gets driven into cut off region. Hence only Q_2 conducts during negative half cycle of the input, producing negative half cycle across the load R_L, as shown in the Fig. 5.34 (a).

Thus for a complete cycle of input, a complete cycle of output signal is developed across the load as shown in the Fig. 5.34 (b)

▶ **Figure 5.34**



(a) Negative half cycle operation **(b) Load voltage waveform**

5.12.1 Mathematical Analysis

All the results derived for push pull transformer coupled class B amplifier are applicable to the complementary class B amplifier. The **only change is that as the output transformer is not present, hence in the expressions, R_L value must be used as it is, instead of R'_L.**

5.12.2 Advantages and Disadvantages

The advantages are :

1. As the circuit is transformerless, its weight, size and cost are less.
2. Due to common collector configuration, impedance matching is possible.
3. The frequency response improves due to transformerless class B amplifier circuit.

The disadvantages are :

1. The circuit needs two separate voltage supplies.
2. The output is distorted to cross-over distortion.

Key Point: *While solving the problems on class B large signal amplifiers, given power is to be assumed maximum unless and otherwise specified and use* $(P_{ac})_{max} = \frac{1}{2}\frac{V_{CC}^2}{R_L}$ *or* $\frac{1}{2}\frac{V_{CC}^2}{R_L'}$ *depending upon type of the circuit.*

If V_{in} *is given then as common collector circuit has unity gain,* $V_{out} = V_{in}$ *and then voltage across* R_L *is same as* V_{in}. *The peak value of* V_{in} *is* V_m *and* $V_m \neq V_{CC}$ *in such a case.*

If supply given is dual such as $V_{CC} = \pm 12$ V, ± 20 V *etc. , it is dual supply version.*

But if supply given is $V_{CC} = 12$ *V, 20 V then it is single supply version and in such a case use* $V_{CC} = \frac{1}{2}$ *(given +* V_{CC} *) i.e* $\frac{12}{2} = 6$ *V,* $\frac{20}{2} = 10$ *V etc. The single supply version is discussed in the section 5.16.*

5.13 Comparison of Push Pull and Complementary Symmetry Circuits

▶ **Table 5.2**

	Push Pull Class B	Complementary Symmetry Class B
1.	Both the transistors are similar either pnp or npn.	Transistors are complementary type i.e. one npn other pnp.
2.	The transformer is used to connect the load as well as input.	The circuit is transformerless.
3.	The impedance matching is possible due to the output transformer.	The impedance matching is possible due to common collector circuit.
4.	Frequency response is poor.	Frequency response is improved.
5.	Due to transformers, the circuit is bulky, costly and heavier.	As transformerless, the circuit is not bulky and costly.
6.	Dual power supply is not required.	Dual power supply is required.
7.	Efficiency is higher than class A.	The efficiency is higher than the push pull.

5.14 Cross-Over Distortion

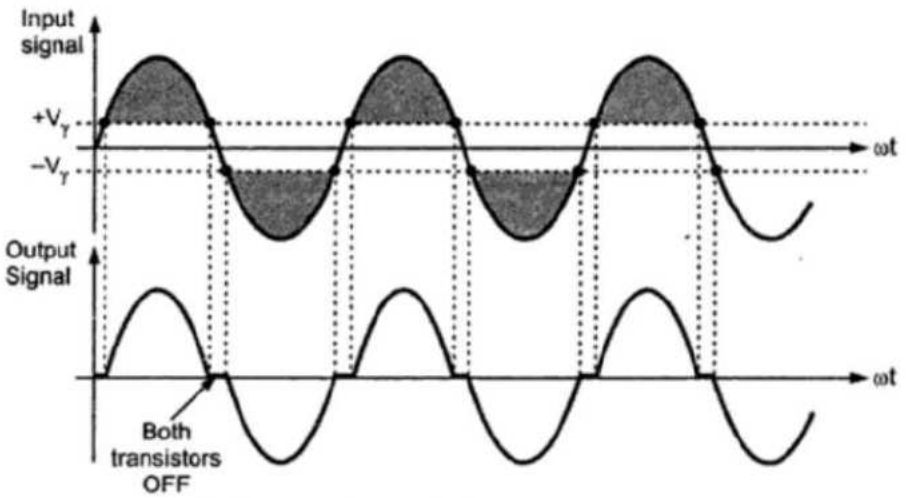
For a transistor to be in active region the base emitter junction must be forward biased. The junction cannot be made forward biased till the voltage applied becomes greater than cut-in voltage (V_γ) of the junction, which is generally 0.7 V for silicon and 0.2V for germanium transistors. Hence as long as the magnitude of the input signal is less than the cut in voltage of the base emitter junction, the collector current remain zero and transistor remains in cut-off region,

Hence there is a period between the crossing of the half cycles of the input signal, for which none of the transistors is active and the output is zero. Hence the nature of the output signal gets distorted and no longer remains same as that of input. Such a distorted output wave form due to cut-in voltage is shown in the Fig. 5.36.

Such a distortion in the output signal is called a **cross-over distortion**. Due to cross-over distortion each transistor conducts for less than a half cycle rather than the complete half cycle. The part of the input cycles for which the two transistors conduct alternately is shown shaded in the Fig. 5.36. The cross-over distortion is common in both the types of class B amplifiers.

▶ **Figure 5.36**

Cross-over distortion



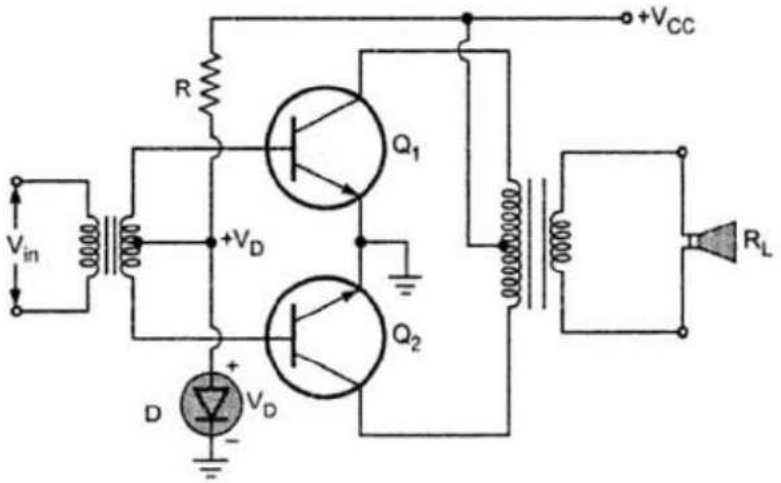
5.15 Elimination of Cross-Over Distortion

To eliminate the cross-over distortion some modifications are necessary, in the basic circuits of the class B amplifiers. The basic reason for the cross over distortion is the cut in voltage of the transistor junction. To overcome this cut-in voltage, a small forward biased is applied to the transistors. Let us see the practical circuits used to apply such forward biased, in the two types of class B amplifiers.

5.15.1 Push Pull Class B Amplifier

▶ Figure 5.37

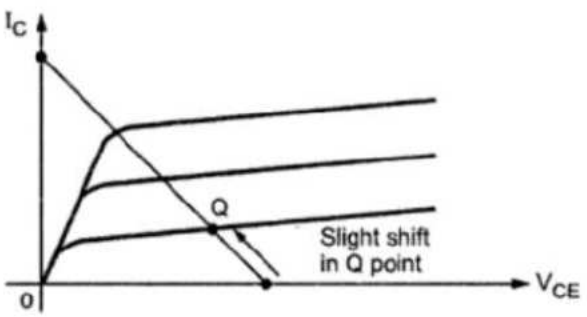
Use of Diode



The forward biased across the base-emitter junction of each transistor is provided by using a diode as shown in the Fig. 5.37.

The drop across the diode D is equal to the cut-in voltage of the base-emitter junction of the transistor. Hence both the transistors conduct for full half cycle, eliminating the cross-over distortion.

▶ Figure 5.38



Due to the forward biased provided to eliminate the cross over distortion, the Q point shifts upwards on the load line as shown in the Fig. 5.38. Hence the operation of the amplifier no longer remains class-B but becomes class AB operation.

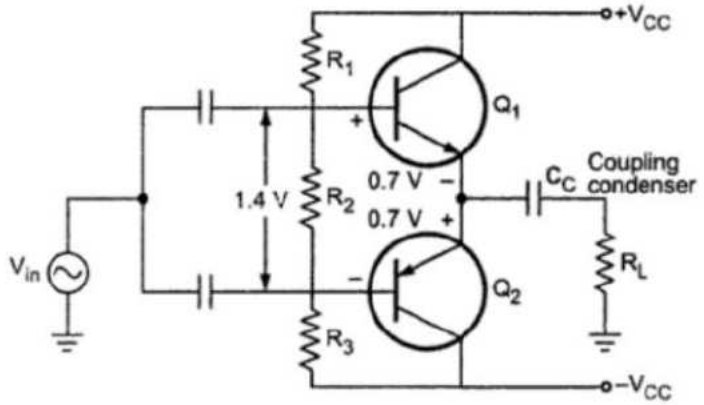
But as the amplifier handles the large signals in the range of volts, compared to these signals the shift in Q point is negligibly small.

Key Point: *For all the practical purposes, the operation is treated as class B operation and all the expression derived are applicable to these modified circuits.*

5.15.2 Complementary Symmetry Class B Amplifier

▶ **Figure 5.39**

Use of potential divider

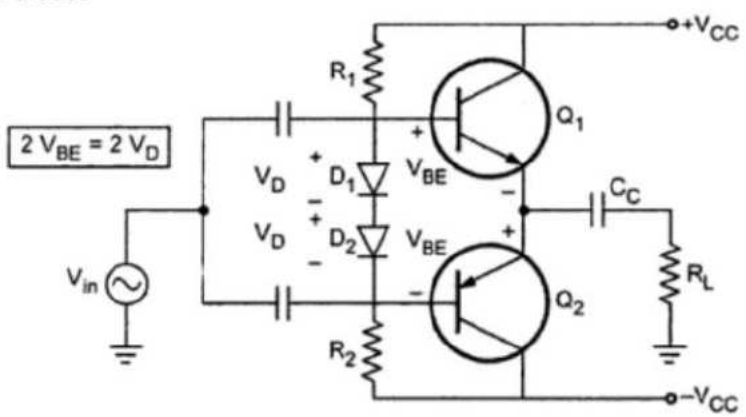


In push pull, transformer coupled type, the drop across forward biased one diode is sufficient, to provide necessary cut in voltage. But in case of complementary symmetry circuit, base emitter junctions of both Q_1 and Q_2, are required to provide a fixed bias. Hence for silicon transistors a fixed bias of 0.7 + 0.7 = 1.4 V is required. This can be achieved by using a potential divider arrangement as shown in the Fig. 5.39.

But in this circuit, the fixed bias provided is fixed equal to say 1.4 V. While the junction cut-in voltage changes with respect to the temperature. Hence there is still possibility of a distortion when there is temperature change. Hence instead of R_2, the two diodes can be used to provide the required fixed bias. As the temperature changes, along with the junction characteristics, the diode characteristics get changed and maintain the necessary biasing required to overcome the cross-over distortion when there is temperature change. The arrangement of the circuit with the two diodes is shown in the Fig. 5.40.

▶ **Figure 5.40**

Use of pair of diodes



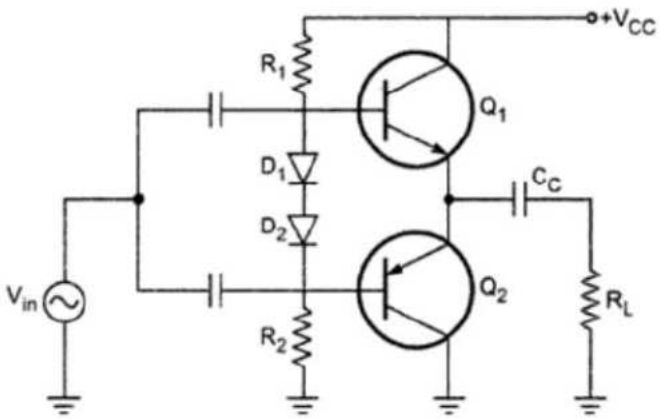
5.16 Complementary Symmetry Single Supply Version

The main disadvantage as seen earlier of complementary amplifier is the use of dual supply. But in practice the circuit can be modified by grounding – V_{CC} terminal. The

resulting circuit is called single supply version of complementary symmetry class B amplifier as shown in the Fig. 5.41.

▶ **Figure 5.41**

Single supply version of complementary symmetry class B amplifier



Key Point: *All the expression derived for dual supply version are still applicable to single supply version.* ***Only change required is that the value of V_{CC} must be taken as $V_{CC}/2$, while calculating the various parameters of the circuit.***

■

UNIT IV
OPERATIONAL AMPLIFIER

Unit - I : Op-Amp Characteristics

The operational amplifier is a multi-terminal device which is internally quite complex. It was originally designed for Computing mathematical functions such as addition, Subtraction, multiplication and Integration. Thus it is named as operational amplifier. and it is abbrevated to op-amp.

with the addition of suitable external Components, op-amp is used for Variety of applications such as amplification, filters, oscillators, Comparators, regulators and others.

Basic information of op-amp

Circuit Symbol

- op-amp has two input terminals and one output terminal.
- The terminal with a (-) sign is called inverting input terminal. and the terminal with (+) sign is Called the non-inverting input terminal.

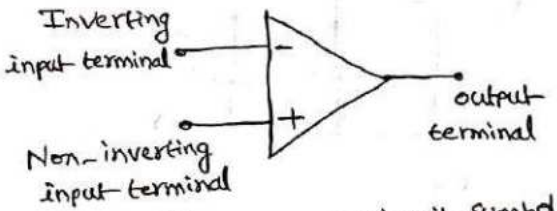


Fig:- op-amp circuit Symbol

Packages

There are three popular types of IC packages.

(1) The Metal Can (TO) Package
(2) Dual-in-line package (DIP)
(3) Flat Package.

Temparature ranges

All Ic's manufactured fall into one of the three basic temperature grades.

(1) Military temperature range : $-55^{\circ}C$ to $+125^{\circ}C$
(2) Industrial temperature range : $-20^{\circ}C$ to $+85^{\circ}C$
(3) Commercial temperature range : $0^{\circ}C$ to $+70^{\circ}C$.

Power Supply Connections

Most linear Ic's use one or more differential amplifier stages and differential amplifiers require both +ve and -ve power supply for proper operation of the circuit.

Two power supplies required for linear IC are usually equal in magnitude ie, ±15V. These power supply voltages must be referenced to a Common point or ground.

Otherwise twice the supply voltage will get applied and it may damage the op-amp.

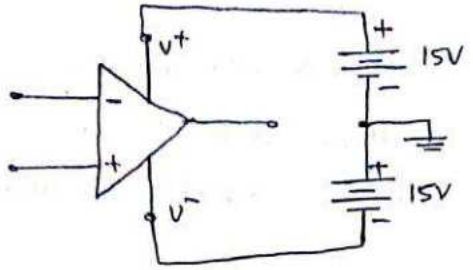
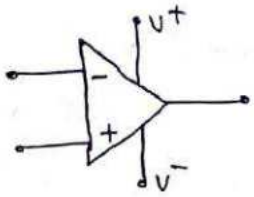


Fig. (a): Power Supply Connections



Fig(b): Circuit symbol showing power supply Connections.

Instead of using two power supplies, one can use a single power supply to obtain V^+ and V^- as shown in fig (c, d and e).

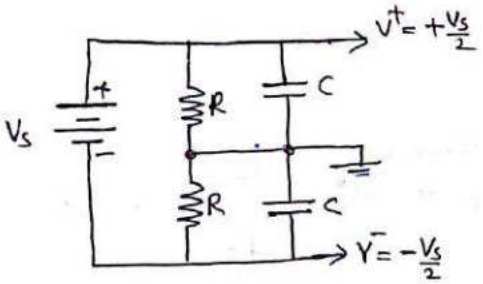


Fig (c).

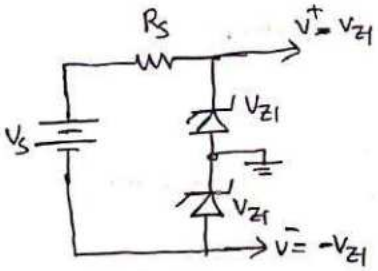


Fig (d).

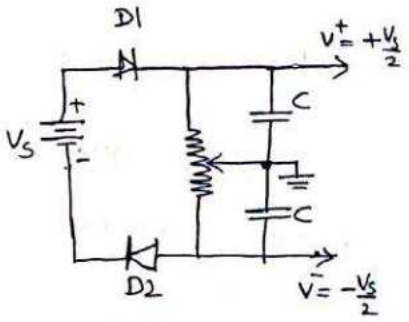


Fig (e):

Fig c,d,e: Different circuits for obtaining +ve and -ve supply voltages for op-amp.

→ In fig (c), resistor R should be greater than 10kΩ so that it does not draw more current from the supply V_S. The two capacitors provide decoupling of the power supply.

→ In fig(d), Zener diodes are used to obtain symmetrical supply voltages. The value of R_S is chosen such that it supplies sufficient current for the Zener diode to operate in breakdown region.

→ In fig(e), potentiometer is used to get equal values of V^+ and V^-. Diodes D1 and D2 protect the IC if +ve and -ve leads of the supply voltage V_S are accidentally reversed.

Ideal op-amp

The op-amp is said to be ideal if it has the following characteristics.

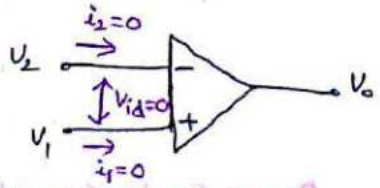


Fig: Ideal op-amp.

(1) open loop gain, $A_{OL} = \infty$
(2) Input Impedance, $R_i = \infty$
(3) output Impedance, $R_o = 0$
(4) Bandwidth, $BW = \infty$
(5) Zero offset i.e, $V_o = 0$ when $V_1 = V_2 = 0$.
(6) Common mode Rejection Ratio, $CMRR = \infty$
(7) Slew rate, $SR = \infty$.

Practical op-amp

In practice we will not get op-amps with ideal characteristics. But practical op-amps can be made to approximate some of the characteristics using -ve feedback arrangement.

The practical 741 – op amp has the following electrical characteristics.

(1) gain : 50,000 to 2,00,000
(2) Input Resistance, R_i : 1MΩ
(3) output Resistance, R_o : 75Ω
(4) offset voltage : 5mV
(5) Band width : 0.437 MHz
(6) CMRR : 70 dB
(7) Slew rate : 0.5 V/μs.

Equivalent Circuit of an op-amp

Equivalent circuit contain input resistance, R_i and thevenin equivalent voltage source AV_{id}, thevenin resistance R_o at the output side.

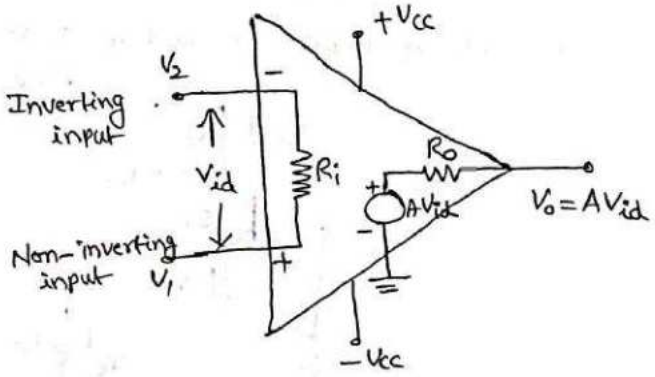


Fig:- Equivalent circuit of an op-amp.

→ From the equivalent circuit, the output voltage is, $\boxed{V_o = AV_{id} = A(V_1 - V_2)}$

where, A = large signal voltage gain
V_{id} = Differential input voltage
V_1 = voltage at +ve terminal
V_2 = voltage at -ve terminal

From the above equation, we can say that op-amp amplifies the difference between two input signals.

Ideal Voltage Transfer Curve

For an op-amp, $V_o = A V_{id}$. If we plot V_o against V_{id}, keeping gain A constant output voltage is directly proportional to the V_{id} only until it reaches saturation voltages and thereafter output voltage remains constant.

→ Transfer curve is ideal because output offset voltage is assumed to be zero.

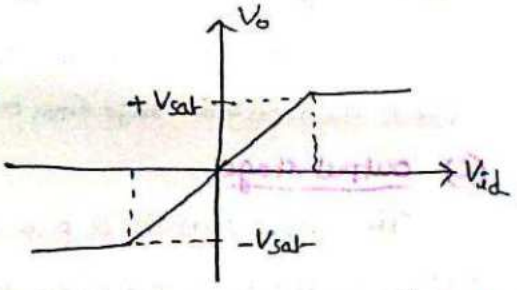


fig:- Ideal voltage transfer curve

Op-amp Internal circuits

IC op-amps usually consists of four cascaded blocks as shown in the figure.

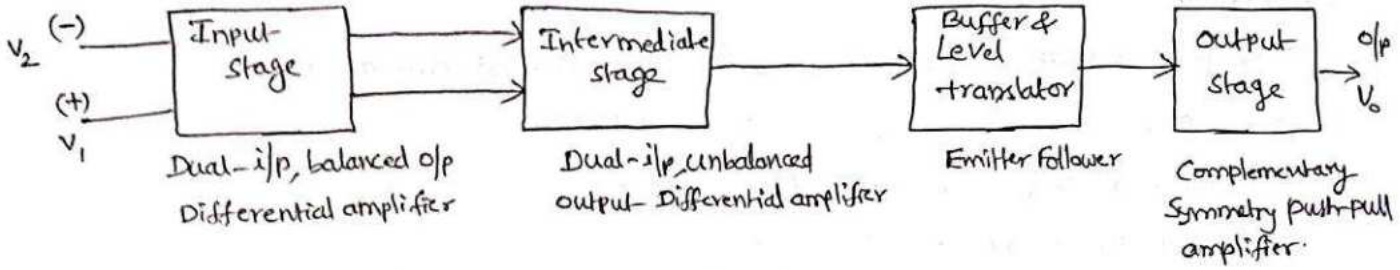


Fig:- Block diagram of an op-amp.

(a) Differential amplifiers

The input stage is the dual input, balanced output differential amplifier. This stage generally provides most of the voltage gain and high input resistance. The intermediate stage is another differential amplifier which is driven from the output of the first stage. In most op-amps, intermediate stage is dual-i/p unbalanced output.

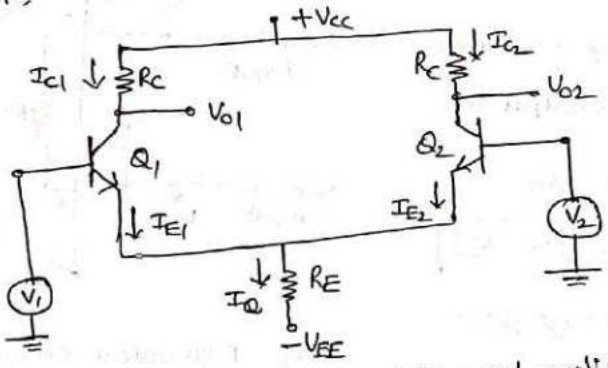


Fig:- The basic differential amplifier.

(b) Level Translator

Because of direct coupling, the dc level rises from stage to stage. The increase in dc level tends to shift the operating point of the next stage. This, inturn, limits the output voltage swing and may even distort the output signal. Therefore level translators are used to shift the dc level to zero before it is applied to next stage.

Level translator also act as a buffer to isolate the high gain stage from output stage.

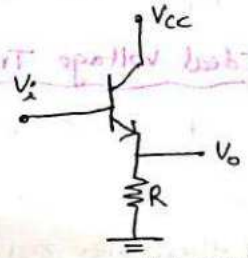


Fig:- Level translator using Emitter follower.

(c) output stage

The output stage is a push-pull amplifier which increases the output voltage swing and raises the current supplying capability of the op-amp.

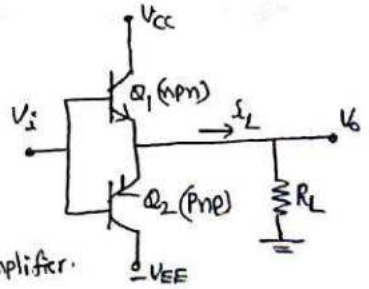


Fig:- push-pull Amplifier.

741 op-amp and its features

741 op-amp has become an industry standard today. The pin configuration of 741 is shown in figure.

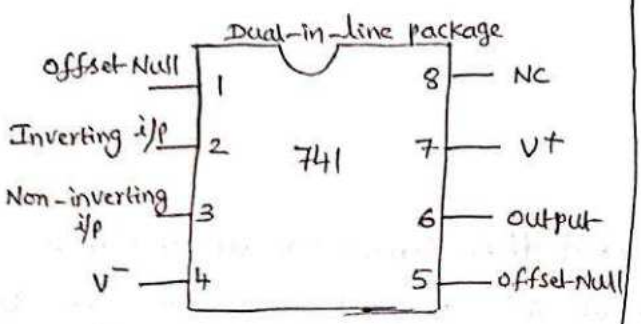


Fig:- Pin configuration

Features

(1) Short circuit protection
(2) Offset Null capability
(3) Low power consumption
(4) No External frequency compensation required
(5) Large common mode and differential voltage ranges
(6) No Latch up problem.

Op-amp parameters

(1) Input offset current

Input offset current I_{io} is the algebraic difference between the currents flowing into inverting and non-inverting terminals.

$$I_{io} = |I_{B1} - I_{B2}|$$

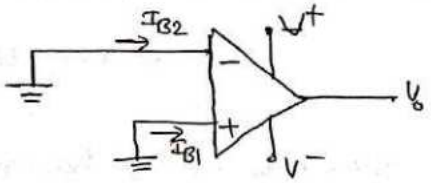


Fig:- Defining input offset current

(2) Input Bias current

Input bias current I_B is the average of the currents that flow into the inverting and non-inverting input terminals of the op-amp.

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

(3) Input offset voltage

Input offset voltage is the voltage that must be applied between the two input terminals of an op-amp to null the output.

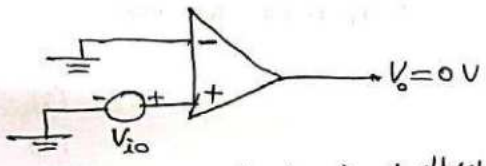


Fig:- Op-amp showing input offset voltage

(4) Common Mode Rejection Ratio (CMRR)

It is defined as the ratio of the differential voltage gain A_d to the common mode voltage gain, A_{CM}.

$$\therefore \quad CMRR = \frac{A_d}{A_{CM}}$$

(5) Supply Voltage Rejection Ratio (SVRR)

Change in op-amp input offset voltage, V_{io} caused by variation in supply voltages is called the supply voltage rejection ratio (or) power supply Rejection Ratio (PSRR). (or) power supply Sensitivity. (PSS).

$$SVRR = \frac{\Delta V_{io}}{\Delta V}$$

(6) Drift

Change in Bias current, offset voltage and offset current with temperature is called. Drift. A circuit carefully nulled at 25°c may not remain same when the temperature rises to 35°c.

offset current drift is expressed in nA/°c and offset voltage drift in mV/°c.

(7) Slew Rate

Slew rate is defined as the maximum rate of change of output voltage per unit time. and is expressed in volts per microsends.

$$\text{Slew rate, } SR = \left.\frac{dV_o}{dt}\right|_{max} \quad V/\mu s$$

Slew rate indicate how rapidly the o/p of an op-amp can change in response to change in the input frequency.

Op-Amp Characteristics

(a) Dc characteristics

An ideal op-amp draws no current from the source and its response also independent of temperature. However, a practical op-amp doesnot work in this way. It takes current from the source into the inputs. Due to mismatch of transistors, two inputs responds differently to voltage and current. These non-ideal dc characteristics that add error to the dc output voltage are

(1) Input bias current
(2) Input offset current
(3) Input offset voltage
(4) Thermal Drift.

(b) Ac Characteristics

For small signal sinusoidal (ac) applications one has to know the ac characteristics such as frequency response and slew Rate.

(i) Frequency Response

Ideally, an op-amp should have an infinite Bandwidth. But in practical op-amp gain decreases at higher frequencies.

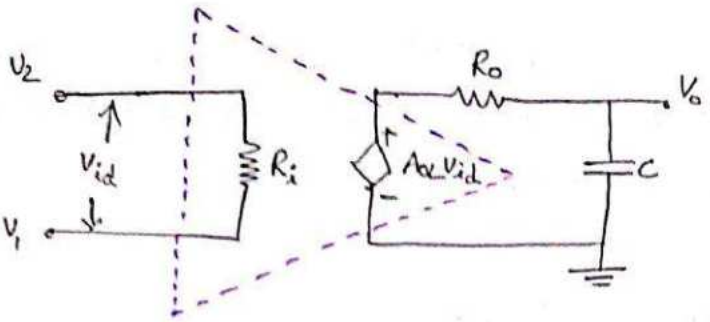


Fig:- High frequency model of an op-amp with single corner frequency

The capacitance is due to internal construction of op-amp. This capacitance causes gain reduction at high frequencies.

From the figure, $V_o = (A_{OL} V_{id}) \left[\frac{1/j\omega C}{R_o + 1/j\omega C}\right] = A_{OL} V_{id} \left[\frac{1}{1+j\omega R_o C}\right]$

$$A = \frac{V_o}{V_{id}} = \frac{A_{OL}}{1+j2\pi f R_o C} = \frac{A_{OL}}{1+j\, f/f_1}, \quad \text{where } f_1 = \frac{1}{2\pi R_o C} = \text{corner frequency}$$

$$|A| = \frac{A_{OL}}{\sqrt{1+(f/f_1)^2}}, \quad \phi = -\tan^{-1}(f/f_1).$$

(i) For $f << f_1$, the magnitude of the gain is $20 \log A_{OL}$

(ii) At $f = f_1$, the gain is 3dB down from the maximum gain. This frequency f_1 is called corner frequency.

(iii) For $f \gg f_1$, the gain reduces at the rate of -20 dB/decade.

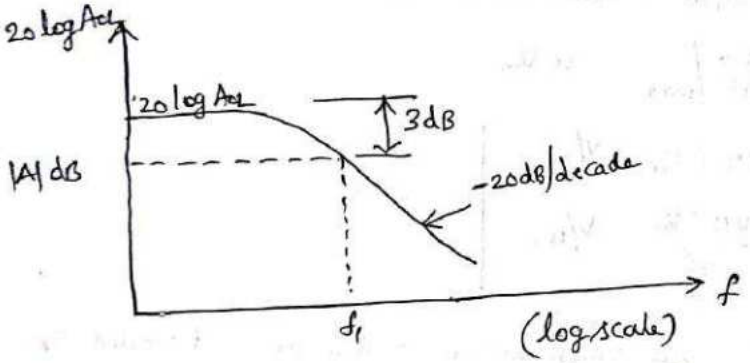
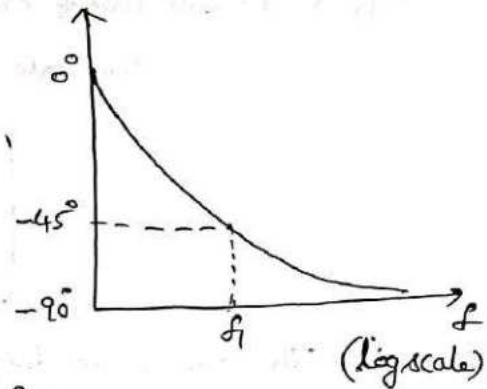


Fig:- Magnitude characteristics



Fig(b):- Phase characteristics for an op-amp

This shows that a maximum of 90° phase change can occur in an op-amp with a single capacitor.

Slew Rate :-

Slew rate is defined as the maximum rate of change of output voltage per unit time.

$$\text{Slew rate, } SR = \left.\frac{dV_o}{dt}\right|_{max} \text{ V/μs.}$$

For Example, a 1V/μs means output rises or fall by 1V in 1 μsecond. (μs).

Causes of slew Rate

There is usually a capacitor within or outside an op-amp prevents the output voltage from responding immediately to a fast changing input. The rate at which the voltage across the capacitor increases is given by

$$\frac{dV_c}{dt} = \frac{I}{C}$$

$$\therefore \boxed{\text{Slew Rate, } SR = \left.\frac{dV_c}{dt}\right|_{max} = \frac{I_{max}}{C}}$$

→ For a sine wave input, the effect of slew rate can be calculated as follows. Consider the voltage follower shown in figure.

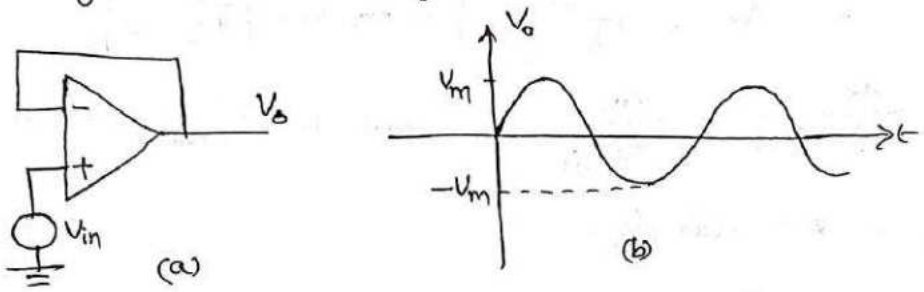


Fig (a) & (b) :- Voltage follower, i/p and o/p waveforms.

If $V_{in} = V_m \sin\omega t$, $V_o = V_{in} = V_m \sin\omega t$

The rate of change of output is given by $\frac{dV_o}{dt} = V_m \omega \cos\omega t$.

The maximum rate of change of output occurs when $\cos\omega t = 1$

$$\therefore \text{Slew rate, } SR = \left.\frac{dV_o}{dt}\right|_{max} = \omega V_m$$

$$\boxed{SR = 2\pi f V_m \ \text{V/s} = \frac{2\pi f V_m}{10^6} \ \text{V/µs}}$$

∴ The maximum frequency, f_{max} at which we can obtain an undistorted o/p voltage of peak value V_m is given by $\boxed{f_{max} = \frac{\text{SlewRate}}{2\pi V_m}}$

Modes of operation

(1) Inverting Amplifier

Input signal V_{in} (ac or dc) is applied to the inverting input terminal through R_1. The o/p voltage is fed back to the inverting i/p terminal through $R_f - R_1$ network.

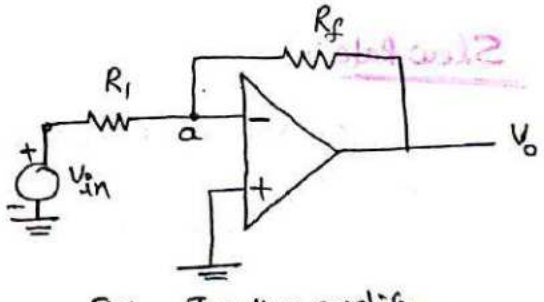


Fig:- Inverting amplifier

The Nodal equation at the node 'a' in figure is

$$\left(\frac{V_a - V_{in}}{R_1}\right) + \left(\frac{V_a - V_o}{R_f}\right) = 0. \quad \rightarrow (1)$$

Since $V_{id} = 0$, voltage at (+) terminal is equal to voltage at (−) ve terminal. Therefore node 'a' is at ground potential. Hence it is called virtual ground. $\therefore V_a = 0$.

Hence eq(1) becomes, $\left(\frac{-V_{in}}{R_1}\right) + \left(\frac{-V_o}{R_f}\right) = 0 \Rightarrow \frac{V_o}{R_f} = \frac{-V_{in}}{R_1}$

$$A_{CL} = \frac{V_o}{V_{in}} = -\frac{R_f}{R_1}$$

The −ve sign indicates a phase shift of 180° between V_{in} and V_o.

(2) Non-inverting Amplifier

Input signal V_{in} (ac or dc) is applied to the non-inverting i/p terminal and feedback is given to the inverting terminal through $R_f - R_1$ network.

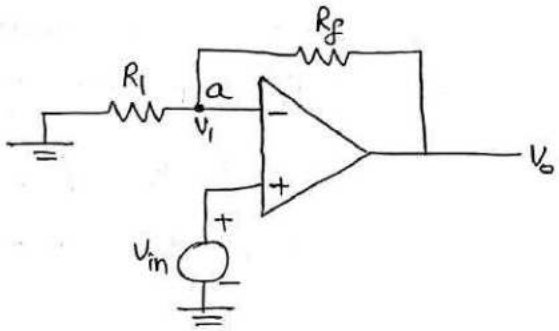


Fig:- Non-inverting Amplifier

Since $V_{id} = 0$, voltage at node 'a' is V_{in}

Nodal equation at the node 'a' in figure is

$$\left(\frac{V_{in} - 0}{R_1}\right) + \left(\frac{V_{in} - V_o}{R_f}\right) = 0$$

$$V_{in}\left[\frac{1}{R_1} + \frac{1}{R_f}\right] = \frac{V_o}{R_f}$$

$$V_{in}\left[\frac{R_f + R_1}{R_1 R_f}\right] = \frac{V_o}{R_f} \Rightarrow \frac{V_o}{V_{in}} = A_{CL} = \left(\frac{R_1 + R_f}{R_1}\right)$$

$$A_{CL} = \frac{V_o}{V_{in}} = 1 + \frac{R_f}{R_1}$$

(3) Voltage Follower (Buffer)

In the non-inverting amplifier if $R_f = 0$ and $R_1 = \infty$, we get a modified circuit shown in figure.

$$\therefore \frac{V_o}{V_{in}} = 1 \Rightarrow V_o = V_{in}$$

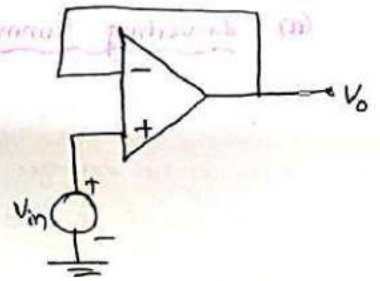


Fig:- Voltage follower.

That is, the o/p voltage is equal to the i/p voltage, both in magnitude and phase. We can say that the o/p voltage follows the i/p voltage. hence the circuit is called a voltage Follower.

It has very high i/p impedance and zero o/p impedance. Thus voltage follower may be used as buffer for impedance matching.

(4) Differential Amplifier

Differential amplifier amplifies the difference between two signals. It is also called Difference amplifier. These are used in instrumentation circuits.

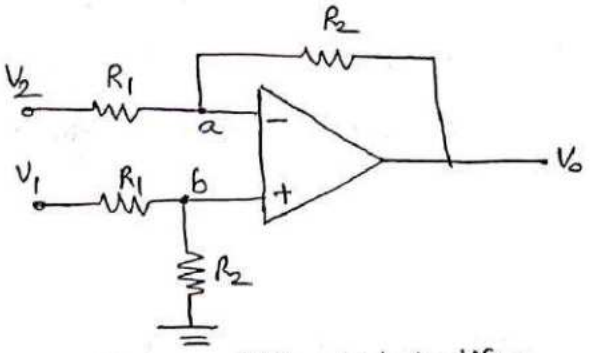


fig:- A differential Amplifier

Since the circuit is having two inputs, we use superposition theorem to find the output voltage.

→ when $V_1 = 0$, configuration becomes an inverting amplifier. hence output due to V_2 only is

$$V_{o2} = -\frac{R_2}{R_1} V_2 \longrightarrow (1)$$

→ when $V_2 = 0$, configuration becomes as non-inverting amplifier having a voltage divider network at the non-inverting input.

$$\therefore V_b = \left(\frac{R_2}{R_1+R_2}\right) V_1$$

$\therefore$ output due to V_1 only is, $V_{o1} = \left(1+\frac{R_2}{R_1}\right) V_b$

$$= \left(1+\frac{R_2}{R_1}\right)\left(\frac{R_2}{R_1+R_2}\right) V_1 = \left(\frac{R_1+R_2}{R_1}\right)\left(\frac{R_2}{R_1+R_2}\right) V_1$$

$$V_{o1} = \frac{R_2}{R_1} V_1 \longrightarrow (2)$$

$\therefore$ Net output voltage, $V_o = V_{o1} + V_{o2}$

$$= \frac{R_2}{R_1} V_1 + \left(\frac{-R_2}{R_1}\right) V_2$$

$$\boxed{V_o = \frac{R_2}{R_1}(V_1 - V_2)}$$

Note:- This circuit is very useful in detecting very small differences in signals.

Applications of op-amp

(a) Inverting Summing Amplifier

Figure shows the summing amplifier with three input voltages V_1, V_2 and V_3, three input resistors R_1, R_2 and R_3 and a feedback resistor R_f.

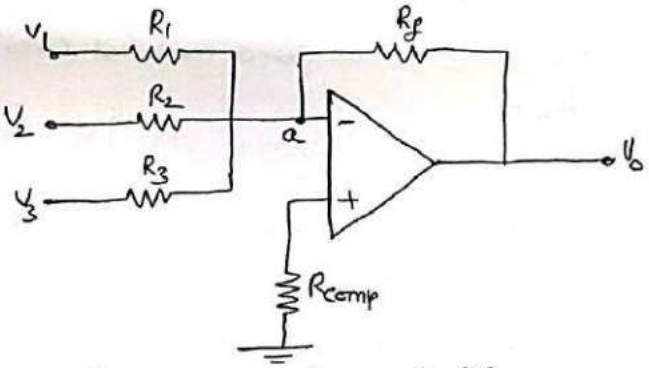


fig:- Inverting Summing Amplifier.

Assuming that the op-amp is ideal, hence the non-inverting i/p terminal is at ground potential. The voltage at node 'a' is Zero.

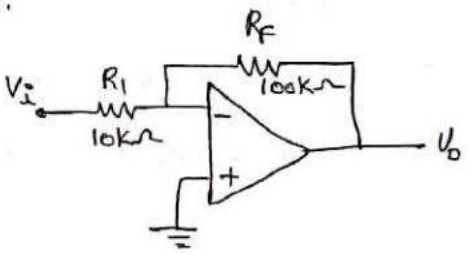
Nodal equation at node 'a' is

$$\left(\frac{0-V_1}{R_1}\right) + \left(\frac{0-V_2}{R_2}\right) + \left(\frac{0-V_3}{R_3}\right) + \left(\frac{0-V_o}{R_f}\right) = 0$$

Problems

① Design an amplifier with a gain of −10 and input resistance of 10 kΩ.

Sol:- Since the gain is negative, it is inverting amplifier.



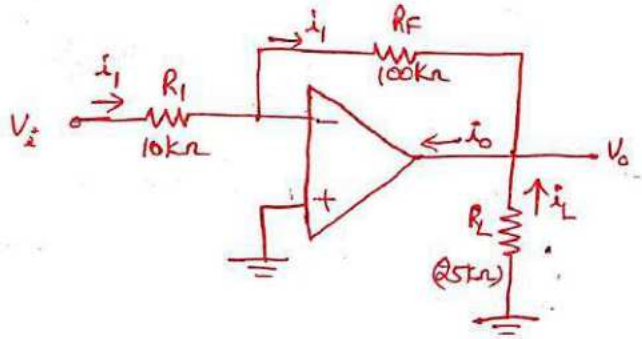
Given that gain, $A_{CL} = -\frac{R_f}{R_1} = -10$

i/p Resistance, $R_1 = 10k\Omega$.

$\therefore \quad A = -\frac{R_f}{R_1}$

$-10 = -\frac{R_f}{10\times10^3} \Rightarrow R_f = 100k\Omega$

② For the circuit shown in figure, $R_1 = 10k\Omega$, $R_F = 100k\Omega$, $V_i = 1V$. A load of 25 kΩ is connected to the o/p terminal. Calculate (i) i_1 (ii) V_o (iii) i_L and (iv) total current i_o into the o/p pin.



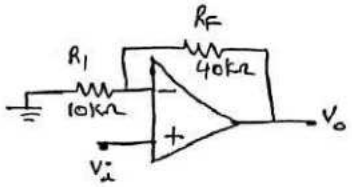
Sol:- (i) $i_1 = \frac{V_i}{R_1} = \frac{1}{10\times10^3} = 0.1mA$

(ii) $V_o = -\frac{R_f}{R_1} V_i = -\frac{100\times10^3}{10\times10^3} \times 1 = -10V$

(iii) $i_L = \frac{V_o}{R_L} = \frac{10}{25\times10^3} = 0.4mA$

(iv) $i_o = i_1 + i_L = 0.1 + 0.4 = 0.5mA$

③ Design an amplifier with a gain of +5.



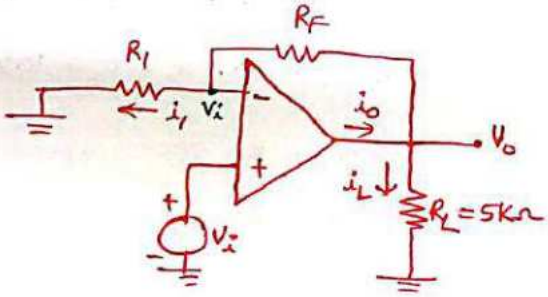
Sol:- Since the gain is +ve, it is non-inverting amplifier.

gain, $A = \left(1 + \frac{R_F}{R_1}\right) = 5$

Let $R_1 = 10k\Omega$, then $5 = \left(1 + \frac{R_F}{10\times10^3}\right)$

$5 - 1 = \frac{R_F}{10\times10^3} \Rightarrow R_F = 4\times10\times10^3 = 40k\Omega$

④ In the circuit shown in figure, $R_1 = 5k\Omega$, $R_F = 20k\Omega$ and $V_i = 1V$. A load resistor of 5 kΩ is connected at the o/p. Calculate (i) V_o (ii) A_{CL} (iii) load current i_L. (iv) the o/p current i_o.



Sol:- (i) $V_o = \left(1 + \frac{R_F}{R_1}\right) V_i = \left(1 + \frac{20\times10^3}{5\times10^3}\right)(1) = 5V$

(ii) $A_{CL} = \frac{V_o}{V_i} = \frac{5}{1} = 5$

(iii) $i_L = \frac{V_o}{R_L} = \frac{5}{5\times10^3} = 1mA$

(iv) $i_o = i_1 + i_L$. , $i_1 = \frac{V_i}{R_1} = \frac{1}{5\times10^3} = 0.2mA$

$i_o = 0.2\times10^{-3} + 1\times10^{-3} = 1.2mA$

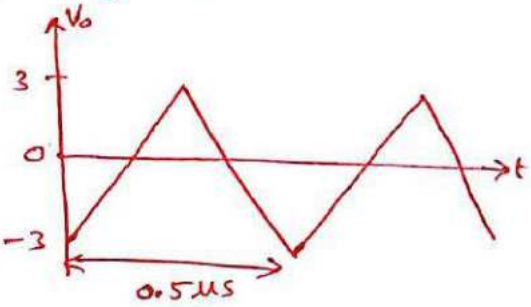
(5) A non-inverting amplifier with a gain of 100 is nulled at 25°C. what will happen to the o/p voltage if the temperature rises to 50°C for an offset voltage drift of 0.15 mV/°C ?

Sol:- Input offset voltage due to temperature rise $= 0.15 \times 10^{-3} (50-25) = 3.75$ mV.

o/p voltage, $V_o = A_{CL} \cdot V_{io}$

$= 100 \times 3.75 \times 10^{-3} = \underline{375 \text{ mV}}$

(6) The o/p of an op-amp voltage follower is a triangular wave shown in figure. what is the slew rate of op-amp?



Sol:- Slew rate is the maximum rate of change of the output.

$\therefore SR = \frac{6}{\left(\frac{0.5}{2}\right) \times 10^{-6}} = 14 \frac{V}{\mu s}$.

(7) A 741C op-amp is used as an inverting amplifier with a gain of 50. The voltage gain vs frequency curve is Flat upto 20KHz. what maximum peak to peak ~~voltage~~ input signal can be applied without distorting the output?

Sol:- Given that, gain = 50, $f = 20$KHz.

For 741C op-amp, Slew rate, $SR = 0.5$ V/μs.

$$SR = \frac{2\pi f V_m}{10^6} \text{ V/μs}$$

$$0.5 = \frac{2\pi \times 20 \times 10^3 \times V_m}{10^6} \Rightarrow \underline{V_m = 3.98 \text{ V peak.}}$$

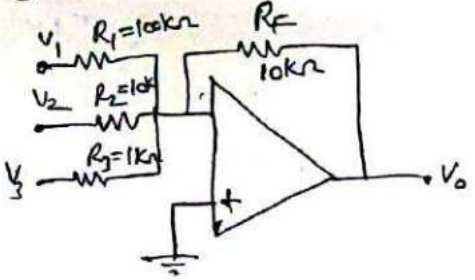
So. $V_o = 2V_m = 7.96$ V

we know gain $= \frac{V_o}{V_i} \Rightarrow V_i = \frac{V_o}{\text{gain}} = \frac{7.96}{50} = \underline{159 \text{ mV}}$

(8) Design an adder circuit using an op-amp to get the o/p Expression as

$V_o = -(0.1V_1 + V_2 + 10V_3)$. where V_1, V_2 and V_3 are the inputs.

Sol:- from the given expression, we can say that circuit is inverting summing Amplifier with o/p, $V_o = -\left[\frac{R_F}{R_1} V_1 + \frac{R_F}{R_2} V_2 + \frac{R_F}{R_3} V_3\right] \rightarrow (1)$



by comparing eq(1) with given V_o, we can write.

$\frac{R_F}{R_1} = 0.1$, $\frac{R_F}{R_2} = 1$, $\frac{R_F}{R_3} = 10$

Let $R_F = 10$KΩ, then $R_1 = \frac{R_F}{0.1} = \frac{10K}{0.1} = 100$KΩ

$R_2 = R_F = 10$KΩ

$R_3 = \frac{R_F}{10} = \frac{10K}{10} = 1$KΩ.

DC Characteristics

An ideal op-amps draws no current from the source. And its response it also independent of temparature. However, a real op-amp does not work in this way. Current is taken from the source into the op-amp inputs. Due to mismatch of transistors two inputs responds differently to current and voltage. These non-ideal dc characteristics that add error components to the dc output voltage are

Input bias current
Input offset current
Input offset voltage
Thermal drift.

AC Characteristics

For small signal sinusoidal (ac) applications, one has to know the ac characteristics such as frequency Response and Slew Rate.

(*) Frequency Compensation

There are two types of compensating techniques

(1) External Compensation
(2) Internal Compensation.

(1) External frequency Compensation

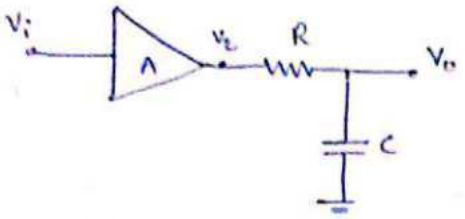
Some type of op-amps are made to be used with externally connected components. These compensating network alters the open loop gain so that the roll of rate is -20dB/ decade over a coide range of frequency.

The common methods for accomplishing this are

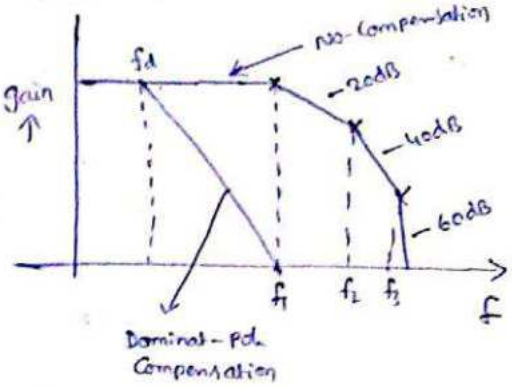
(a) Dominant pole compensation
(b) pole-zero Compensation.

(a) Dominant Pole Compensation

For the uncompensated transfer function of the op-amp, introduce a dominant pole by adding RC network in series with the op amp as shown in fig.



fig(a): Dominat pole compensation



fig(b): Grain Vs frequency curve for dominant pole compensation

$$\frac{V_o}{V_2} = \frac{\frac{1}{j\omega C}}{R+\frac{1}{j\omega C}} = \frac{1}{1+j\omega RC}$$

$$= \frac{1}{1+j\,f/f_d}, \text{ where } f_d = \frac{1}{2\pi RC}$$

$\frac{V_2}{V_i}$ is the open loop gain $= \dfrac{A_{OL}}{(1+jf/f_1)(1+j\frac{f}{f_2})(1+j\frac{f}{f_3})}$

$$\therefore \quad \frac{V_o}{V_i} = \frac{V_o}{V_2} \cdot \frac{V_2}{V_i}$$

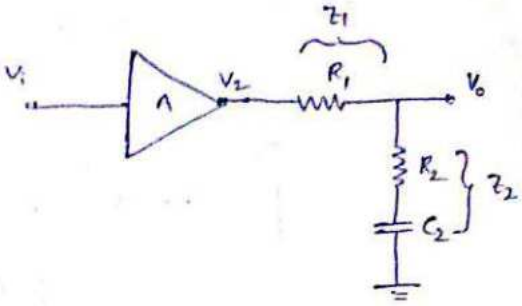
$$= \frac{A_{OL}}{(1+jf/f_d)(1+jf/f_1)(1+jf/f_2)(1+jf/f_3)}, \text{ where } f_d < f_1 < f_2 < f_3$$

The capacitance C is choosen so that the modified loop gain drops to 0 dB with a slope of -20dB/decade at a frequency where poles of uncompensated transfer function contribute negligible phase shift.

The Disadvantage of this method is it reduces the bandwidth drastically. But the noise immunity of the system is improved.

(b) Pole - Zero Compensation

Here the uncompensated transfer function is altered by adding both pole and zero as shown in fig. The zero should be at higher frequency than pole.



The transfer function of the Compensating network alone is

$$\frac{V_o}{V_2} = \frac{Z_2}{Z_1+Z_2} = \frac{R_2 + \frac{1}{j\omega C_2}}{R_1+R_2+\frac{1}{j\omega C_2}}$$

$$= \frac{1+j\omega R_2 C_2}{1+j\omega(R_1+R_2)C_2} = \frac{1+jf/f_1}{1+jf/f_p}$$

where $f_1 = \frac{1}{2\pi R_2 C_2}$

$f_p = \frac{1}{2\pi(R_1+R_2)C_2}$

The Compensating network is designed to produce a zero at the first corner frequency f_1 of the uncompensated transfer function. The zero will cancel the effect of the pole at f_1.

Overall transfer function is

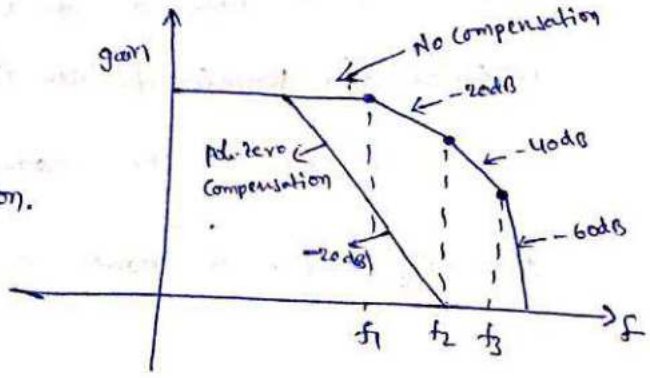
$$\frac{V_o}{V_i} = \frac{V_o}{V_2}\cdot\frac{V_2}{V_i} = \frac{A_{OL}}{(1+j\frac{f}{f_1})(1+j\frac{f}{f_2})(1+jf/f_3)} \cdot \frac{(1+j\frac{f}{f_1})}{(1+jf/f_p)}$$

$$= \frac{A_{OL}}{(1+jf/f_p)(1+jf/f_2)(1+jf/f_3)}$$

where $0 < f_p < f_1 < f_2 < f_3$

The pole of the compensating network is selected so that the Compensated transfer function passes through 0 dB at the second corner frequency f_2.

Advantage of this method is Bandwidth improved Compared to dominant-pole compensation.



(2) ~~Internally~~ Compensated

(2) Internal Compensation

Internally Compensated op-amps are called Compensated op-amps. They are stable regardless of the value of closed loop gain and with out any external Compensating network.

Slew Rate

The slew rate is defined as the rate of change of output voltage per unit time. It is usually specified in V/μs.

$$SR = \left.\frac{dV_o}{dt}\right|_{maximum} \quad V/\mu s.$$

for example, a 1V/μs means output rises or falls by 1V in 1 μsecond.

Causes of Slew Rate

There is usually a capacitor within or outside an op amp prevents the output voltage from responding immediately to a fast changing input. The rate at which the voltage across the capacitor 'C' increases is given by

$$\frac{dV_o}{dt} = \frac{I}{C}$$

$$\therefore \quad SR = \left.\frac{dV_c}{dt}\right|_{max} = \frac{I_{max}}{C}$$

$Q = CV$

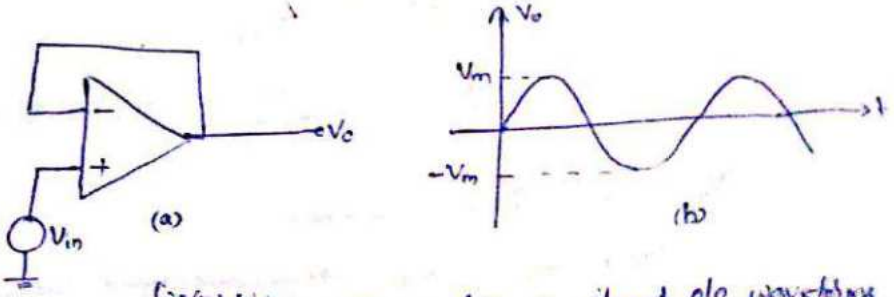
$It = CV$

$I = C\frac{dv}{dt}$

$\frac{dv}{dt} = \frac{I}{C}$

~~Slew Rate for Sinusoid~~.

for a Sine wave input, the effect of slew rate can be Calculated as follows. Consider the voltage follower shown in fig.



fig(a) & (b): voltage follower, i/p and o/p waveforms

5-7 EFFECT OF VARIATION IN POWER SUPPLY VOLTAGES ON OFFSET VOLTAGE

In the preceding section we studied the effect of input offset voltage and input offset current thermal drifts on the output voltage of inverting as well as noninverting amplifiers. As we have mentioned before, the V_{io}, I_{io}, and I_B values are also susceptible to the changes in the supply voltages $+V_{CC}$ and $-V_{EE}$. Obviously, because the op-amp is capable of amplifying dc inputs, it is sensitive to changes in its supply voltages. This section is concerned with the effect of variation in supply voltages $+V_{CC}$ and $-V_{EE}$ on the values of V_{io}, I_{io}, and I_B and, in turn, the effect of changes in V_{io}, I_{io}, and I_B on output offset voltage.

Once we select the specific values for supply voltages $+V_{CC}$ and $-V_{EE}$ in a given op-amp amplifier, we do not change them deliberately. However, sometimes these voltages may change as a result of poor regulation and filtering. A poorly regulated power supply gives different values depending on the size and type of load connected to it. On the other hand, a poorly filtered power supply has a ripple voltage riding on some specific dc level.

Figure 5-27(a) shows the input bias current versus supply voltage curve for the LH0001 op-amp. A glance at output offset voltage V_{ol_B} [Equation (5-16)] reveals that for a given value of R_F any change in I_B causes a change in V_{ol_B}. However, you will recall that we can use the R_{OM} resistor to minimize the effect of I_B or of changes in it on the output offset voltage V_{ol_B}.

Even though input bias currents change due to the change in supply voltages, the input offset current should remain relatively constant because it is

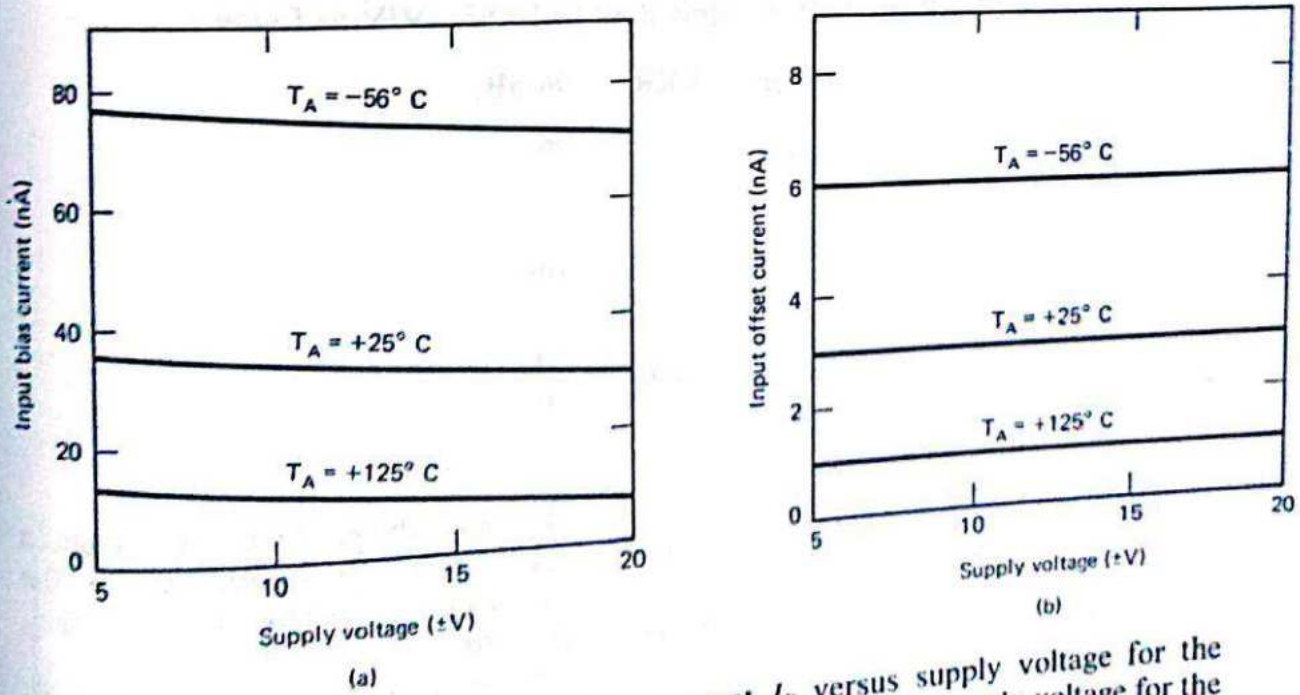


Figure 5–27 (a) Input bias current I_B versus supply voltage for the LH0001 op-amp. (b) Input offset current I_{io} versus supply voltage for the LH0001 op-amp. (Courtesy of National Semiconductor.)

the absolute value of the difference between two input bias currents [see Figure 5-27(b)]. Thus, in practice, if we use a proper value of the R_{OM} resistor in a given amplifier circuit, there will be a negligible change in the current-generated output offset voltage due to the change in supply voltages. Therefore, manufacturers do not furnish curves like those in Figure 5-27 for all op-amps.

Recall that the supply voltages change because of poor regulation and filtering. For a given op-amp any change in the values of the supply voltages results in a change in the input offset voltage, which in turn causes a change in the output offset voltage. The change in op-amp's input offset voltage caused by variations in the supply voltages is generally specified on the data sheets by a variety of terms: The input offset voltage sensitivity, the power supply rejection ratio, the power supply sensitivity, and the supply voltage rejection ratio are some of them. All these terms are equivalent since they convey the same information. These terms are expressed either in microvolts per volt or in decibels. For example, the supply voltage rejection ratio (SVRR) for the μA741 is $\Delta V_{io}/\Delta V = 150$ μV/V maximum, and it is typically 20 log $(\Delta V/\Delta V_{io}) = 96$ dB for the LM307, where ΔV is the change in supply voltages $+V_{CC}$ and $-V_{EE}$, and ΔV_{io} is the resulting change in the input offset voltage.

Given a supply voltage rejection ratio in microvolts per volt, we can obtain an equivalent value in decibels (dB), or vice versa. For instance, SVRR $(\Delta V_{io}/\Delta V)$ of 150 μV/V is equivalent to

$$20 \log \left(\frac{1}{\text{SVRR}}\right) = 20 \log \left(\frac{1}{\Delta V_{io}/\Delta V}\right) = 20 \log \left(\frac{1}{150\ \mu\text{V/V}}\right) = 20 \log \left(\frac{10^6}{150}\right)$$

$$= 76.48 \text{ dB}$$

Similarly, an SVRR of 96 dB is equivalent to 15.85 μV/V as follows.

$$20 \log(1/\text{SVRR}) = 96 \text{ dB},$$

$$\log \left(\frac{1}{\text{SVRR}}\right) = \frac{96}{20}$$

$$\frac{1}{\text{SVRR}} = 10^{4.8}$$

$$\text{SVRR} = \frac{1}{10^{4.8}}$$

$$= 15.85\ \mu\text{V/V}$$

Note that the higher the value of SVRR in decibels, the lower is the change in input offset voltage due to the change in supply voltages or, in other words, the lower the value of SVRR in μV/V, the better for op-amp performance. In fact, ideally the value of SVRR in μV/V should be zero.

Now we find for a given amplifier the change in output voltage due to the supply voltage rejection ratio. Refer again to the completely compensated inverting amplifier circuit shown in Figure 5-24. Let us assume that the amplifier is

nulled initially. Suppose that, after the circuit is in operation for a while, the supply voltages change in value due to poor regulation. We know that any change in the supply voltages results in a change in the input offset voltage. And, according to Equation (5-8), any change in input offset voltage results in a change in the output offset voltage. Therefore, using Equation (5-8) we can establish a relationship between the change in output offset voltage and SVRR as follows:

$$V_{oo} = \left(1 + \frac{R_F}{R_1}\right) V_{io} \tag{5-8}$$

where $(1 + R_F/R_1)$ is a constant for given values of R_1 and R_F. Therefore, the average change in V_{oo} per unit change in supply voltages can be

$$\frac{\Delta V_{oo}}{\Delta V} = \left(1 + \frac{R_F}{R_1}\right)\left(\frac{\Delta V_{io}}{\Delta V}\right) \tag{5-33}$$

Multiplying both sides of Equation (5-33) by ΔV, we get

$$\Delta V_{oo} = \left(1 + \frac{R_F}{R_1}\right)\left(\frac{\Delta V_{io}}{\Delta V}\right) \Delta V \tag{5-34}$$

where ΔV_{oo} = change in output offset voltage (volts)
ΔV = change in supply voltages $+V_{CC}$ and $-V_{EE}$
$\frac{\Delta V_{io}}{\Delta V}$ = supply voltage rejection ratio (μV/V)

Remember that ΔV_{oo} is a dc voltage, and it could be either positive or negative. Thus all practical op-amps are affected by changes in the supply voltages, and therefore regulated supplies are recommended.

EXAMPLE 5-11

The amplifier in Figure 5-28(b) is nulled when the low dc supply is 20 V [see Figure 5-28(a)]. Because of poor regulation, low dc voltage varies with time from 18 V to 22 V. Determine (a) the change in the output offset voltage caused by the change in supply voltages, and (b) the output voltage V_o if V_{in} = 10 mV dc. The op-amp is the LM307 with SVRR = 96 dB.

SOLUTION (a) The variation in low dc voltage from 18 V to 22 V, compared to its desired value of 20 V ($+V_{CC} = +10$ V and $-V_{EE} = -10$ V) implies that the change in supply voltages $\Delta V = 2$ V. The supply voltage rejection ratio (SVRR) equivalent to 96 dB is 15.85 μV/V. That is,

$$\frac{\Delta V_{io}}{\Delta V} = 15.85\ \mu\text{V/V}$$

6-10.4 *Difference between Bandwidth, Transient Response, and Slew Rate*

Table 6-2 is a summary of three important ac parameters of the op-amp: bandwidth, transient response, and slew rate. A clear idea of the differences between these parameters is important in ac applications.

TABLE 6-2 SUMMARY OF AC PARAMETERS

Bandwidth	Transient response	Slew rate
A small-signal phenomenon	A small-signal phenomenon	A large-signal phenomenon
Band of frequencies for which the gain remains constant	That part of the total response before the response reaches a steady state	The maximum time rate of change of the output voltage
Depends on compensating components and closed-loop gain	Composed of overshoot and rise time; rise time is related to bandwidth and overshoot is a measure of stability	Slew rate limiting depends on both frequency and amplitude; often increases with closed-loop gain and power supply voltages
If exceeded, results in a reduction of output voltage	Affects settling time	If exceeded, results in distortion

SUMMARY

1. Frequency response is the manner in which the gain magnitude and the phase angle between the input and output respond to different frequencies.
2. Compensating networks are used to control the phase shift and thus improve the stability of the op-amps. These networks are typically composed of resistors and capacitors. The compensating network is either designed into the circuit or is added at designated terminals.
3. In internally compensated op-amps, the compensating network is designed into the circuit. On the other hand, a compensating network is added externally in noncompensated op-amps. Generally, open-loop noncompensated op-amps have wider bandwidths than those of compensated op-amps.
4. Because of capacitances within the op-amp, the gain decreases and the phase shift between input and output voltages increases as frequency increases.
5. The open-loop gain of the op-amp is relatively constant at frequencies below [illegible] but successively decreases at a rate of −20 dB/decade

UNIT V
APPLICATIONS OF OP-AMPS AND SPECIAL ICs

(4) Differential Amplifier

Differential amplifier amplifies the difference between two signals. It is also called Difference amplifier. These are used in instrumentation circuits.

Since the circuit is having two inputs, we use Superposition theorem to find the output voltage.

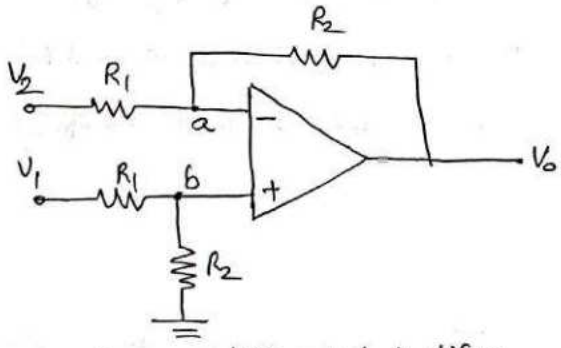


fig:- A differential Amplifier

→ when $V_1 = 0$, Configuration becomes an inverting amplifier. hence output due to V_2 only is

$$V_{o2} = -\frac{R_2}{R_1} V_2 \rightarrow (1)$$

→ when $V_2 = 0$, Configuration becomes as non-inverting amplifier having a voltage divider network at the non-inverting input.

$$\therefore V_b = \left(\frac{R_2}{R_1+R_2}\right) V_1 .$$

$$\therefore \text{output due to } V_1 \text{ only is, } V_{o1} = \left(1+\frac{R_2}{R_1}\right) V_b$$

$$= \left(1+\frac{R_2}{R_1}\right)\left(\frac{R_2}{R_1+R_2}\right)V_1 = \left(\frac{R_1+R_2}{R_1}\right)\left(\frac{R_2}{R_1+R_2}\right) V_1$$

$$V_{o1} = \frac{R_2}{R_1} V_1 \rightarrow (2)$$

$$\therefore \text{Net output voltage, } V_o = V_{o1} + V_{o2}$$

$$= \frac{R_2}{R_1} V_1 + \left(\frac{-R_2}{R_1}\right) V_2$$

$$\boxed{V_o = \frac{R_2}{R_1}(V_1 - V_2)}$$

Note:- This circuit is very useful in detecting very small differences in signals.

Applications of op-amp

(a) Inverting Summing Amplifier

Figure shows the Summing amplifier with three input voltages V_1, V_2 and V_3, three input resistors R_1, R_2 and R_3 and a feedback resistor R_f.

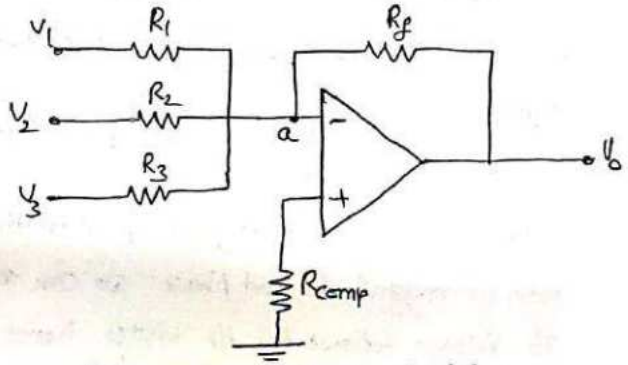


fig:- Inverting Summing Amplifier

Assuming that the op-amp is ideal, hence the non-inverting i/p terminal is at ground Potential. The voltage at node 'a' is Zero.

Nodal equation at node 'a' is

$$\left(\frac{0-V_1}{R_1}\right) + \left(\frac{0-V_2}{R_2}\right) + \left(\frac{0-V_3}{R_3}\right) + \left(\frac{0-V_o}{R_f}\right) = 0$$

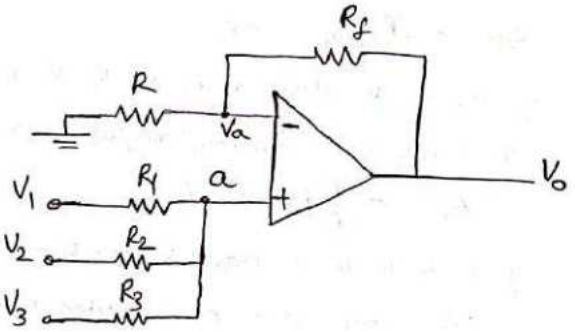
$$\frac{V_o}{R_f} = -\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right) \Rightarrow \boxed{V_o = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right]}$$

⇒ when $R_1 = R_2 = R_3 = R_f$, we have $V_o = -(V_1+V_2+V_3)$ i.e, o/p voltage is the inverted sum of the inputs

⇒ when $R_1 = R_2 = R_3 = 3R_f$, $V_o = -\left(\frac{V_1+V_2+V_3}{3}\right)$ i.e, output voltage is the average of the input signals.

(b) Non-inverting Summing Amplifier

The voltage at (+) i/p terminal and (−) i/p terminal is V_a.



The nodal equation at node 'a' is given by

$$\left(\frac{V_a - V_1}{R_1}\right) + \left(\frac{V_a - V_2}{R_2}\right) + \left(\frac{V_a - V_3}{R_3}\right) = 0$$

$$V_a\left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right] = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}$$

$$V_a = \frac{\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)}{\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)}$$

The op-amp is in non-inverting configuration. $\therefore V_o = \left(1 + \frac{R_f}{R}\right)V_a$

$$\boxed{V_o = \left(1 + \frac{R_f}{R}\right)\frac{\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)}{\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)}}$$

⇒ when $R_1 = R_2 = R_3 = R = \frac{R_f}{2}$, then $V_o = V_1 + V_2 + V_3$, i.e, o/p is the weighted sum of i/p's.

(C) Subtractor

A basic differential amplifier can be used as a subtractor if all the resistors are equal in value.

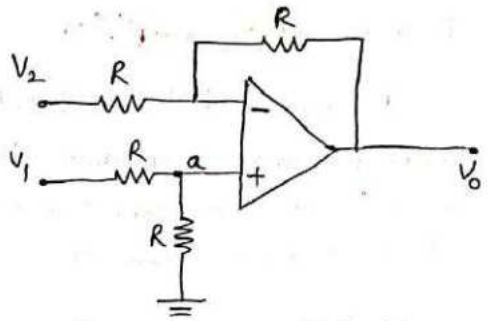


Fig:- op-amp as Subtractor.

The o/p voltage can be obtained by using Super position principle.

⇒ if V_1 is acting alone, and $V_2 = 0$, then circuit is in non-inverting configuration.

So $V_o = \left(1 + \frac{R}{R}\right)V_a$, where $V_a = \left(\frac{R}{R+R}\right)V_1 = \frac{V_1}{2}$

$\therefore V_{o1} = 2\left(\frac{V_1}{2}\right) = V_1$.

⇒ if V_2 is acting alone, and $V_1 = 0$, then circuit is in inverting configuration,

$$\therefore V_{o2} = -\left(\frac{R}{R}\right)V_2 = -V_2.$$

The output voltage V_o due to both the inputs is $V_o = V_{o1} + V_{o2}$

$$\boxed{V_o = V_1 - V_2}$$

(d) Adder – Subtractor

It is possible to perform addition and subtraction simultaneously with a single op-amp using the circuit shown in figure.

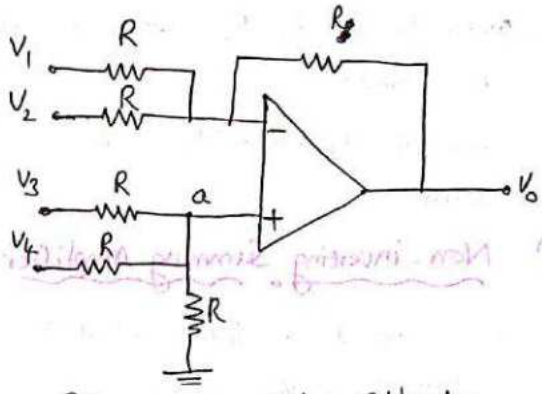


Fig:- op-amp Adder – Subtractor

The o/p voltage V_o can be obtained by Super position principle.

⇒ output due to V_1 alone, make $V_2 = V_3 = V_4 = 0$.

The circuit is in inverting configuration with

$$V_{o1} = -\left(\frac{R}{R}\right) V_1 = -V_1$$

⇒ o/p due to V_2 alone, make $V_1 = V_3 = V_4 = 0$

The circuit is in inverting configuration with

$$V_{o2} = -\left(\frac{R}{R}\right) V_2 = -V_2$$

⇒ o/p due to V_3 alone, make $V_1 = V_2 = V_4 = 0$

The circuit is in non-inverting configuration with output $V_{o3} = \left(1 + \frac{R}{R/2}\right) V_a$,

where $V_a = \left(\frac{R/2}{R + R/2}\right) V_3 = \frac{V_3}{3}$

$$\therefore \quad V_{o3} = 3V_a = 3 \cdot \left(\frac{V_3}{3}\right) = V_3$$

⇒ o/p due to V_4 alone, make $V_1 = V_2 = V_3 = 0$

The circuit is in non-inverting configuration with output $V_{o4} = \left(1 + \frac{R}{R/2}\right) V_a = 3V_a$.

where $V_a = \left(\frac{R/2}{R + R/2}\right) V_4 = \frac{V_4}{3}$.

$$\therefore \quad V_{o4} = 3 \cdot \left(\frac{V_4}{3}\right) = V_4$$

Thus, the o/p voltage V_o due to all four inputs is $V_o = V_{o1} + V_{o2} + V_{o3} + V_{o4}$

$$V_o = -V_1 - V_2 + V_3 + V_4$$

$$\boxed{V_o = (V_3 + V_4) - (V_1 + V_2)}$$

Instrumentation Amplifier

In number of industrial and consumer applications, it is required to measure and control physical quantities such as temperature, humidity, light intensity etc. These quantities are usually measured with transducers. The o/p of the transducer is amplified so that it can drive the indicator or display system. This function is performed by an instrumentation amplifier.

Features:

(1) High gain Accuracy
(2) High CMRR
(3) High gain stability
(4) Low DC offset
(5) Low output impedance.

Figure shows the instrumentation amplifier with 3 – op-amps.

The voltage at (+) terminal of op-amp A3 is $\frac{R_2 V_1'}{R_1 + R_2}$. Using superposition theorem, output

Voltage, $V_o = -\frac{R_2}{R_1} V_2' + \left(1+\frac{R_2}{R_1}\right)\left(\frac{R_2 V_1'}{R_1+R_2}\right) = \frac{R_2}{R_1}(V_1'-V_2')$ ... → (1)

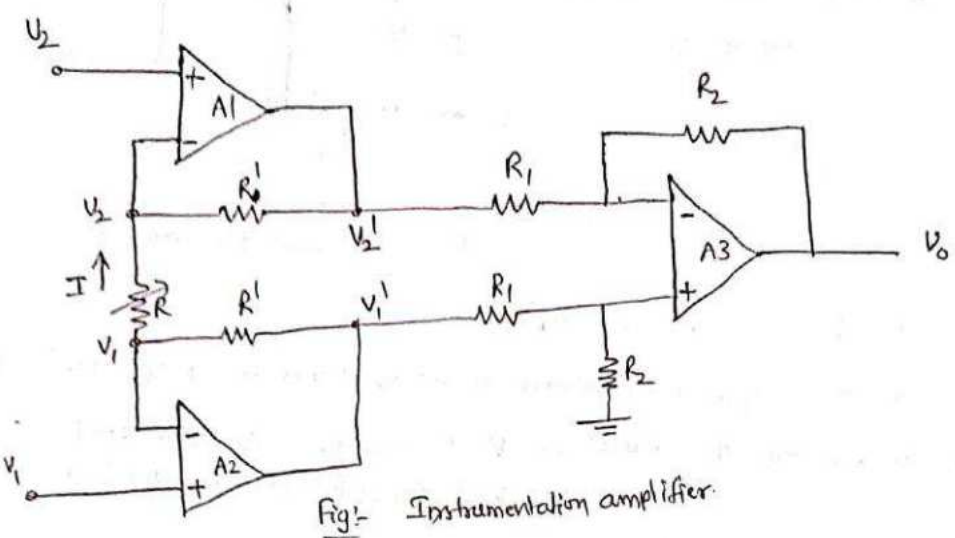


Fig:- Instrumentation amplifier

Since, no current flows into op-amp, the current I flowing in R is $I = \left(\frac{V_1-V_2}{R}\right)$ and same current passes through the resistor R'.

$$V_1' = IR' + V_1 = \frac{R'}{R}(V_1-V_2) + V_1 \quad \rightarrow (2)$$

$$V_2' = -IR' + V_2 = -\frac{R'}{R}(V_1-V_2) + V_2 \rightarrow (3)$$

Substitute eq(2) and (3) in eq(1), we obtain

$$V_o = -\frac{R_2}{R_1}\left(-\frac{R'}{R}(V_1-V_2)+V_2\right) + \left(\frac{R_1+R_2}{R_1}\right)\left(\frac{R_2}{R_1+R_2}\right)\left(\frac{R'}{R}(V_1-V_2)+V_1\right)$$

$$= \frac{R_2}{R_1}\frac{R'}{R}(V_1-V_2) - \frac{R_2}{R_1}V_2 + \frac{R_2}{R_1}\frac{R'}{R}(V_1-V_2) + \frac{R_2}{R_1}V_1$$

$$= \frac{R_2}{R_1}(V_1-V_2) + 2\frac{R_2}{R_1}\frac{R'}{R}(V_1-V_2) = \frac{R_2}{R_1}\left(1+\frac{2R'}{R}\right)(V_1-V_2)$$

The differential gain of this instrumentation amplifier can be varied by replacing the resistor R by a potentiometer.

AC Amplifier

Inverting and non-inverting amplifiers responds to both ac and dc signals. However it one wants to get the ac frequency response of an op-amp or if the ac i/p signal is superimposed with dc level, it is necessary to block the Dc component. This is achieved using an AC amplifier.

(a) Inverting AC amplifier

The capacitor C blocks the dc component of the i/p.

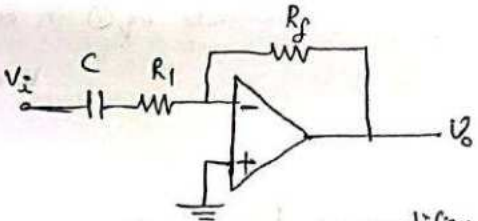


Fig:- Inverting AC amplifier

$$V_o = \left[\frac{-R_f}{R_1 + \frac{1}{j\omega C}}\right] V_i$$

$$A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_1}\left[\frac{1}{1+\frac{1}{j\omega R_1 C}}\right]$$

The Lower 3-dB frequency, $f_L = \frac{1}{2\pi R_1 C}$.

At mid-frequencies, capacitor C behaves as a short ckt and therefore $A_{CL} = -\frac{R_f}{R_1}$

(b) Non-inverting AC amplifier

Capacitor C_1 blocks dc component of i/p signal. Therefore in the o/p we get AC signal only..

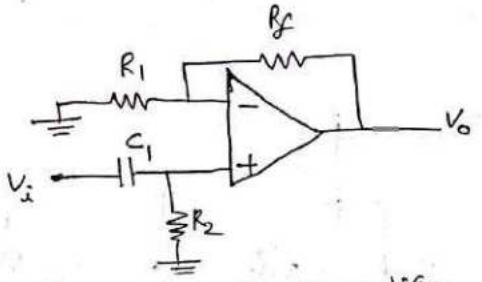


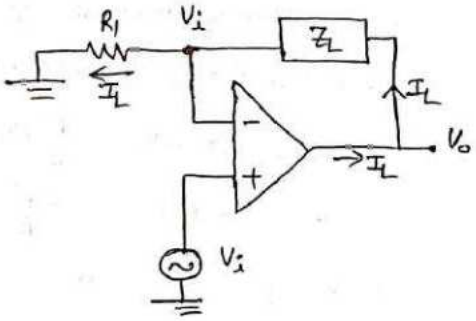
Fig:- Non-inverting AC amplifier

Voltage to current Converter (Transconductance Amplifier)

In many applications, one may have to convert a voltage signal to a proportional output current.. For this there are two types of circuits: (1) V-I Converter with floating load
(2) V-I Converter with grounded load.

(a) V-I Converter with Floating Load

Figure shows V-I Converter in with load resistor is floating (not connected to ground).



From figure, $\boxed{i_L = \frac{V_i}{R_1}}$

i.e, the i/p voltage V_i is converted into an o/p current i_L.

(b) V-I Converter with grounded Load

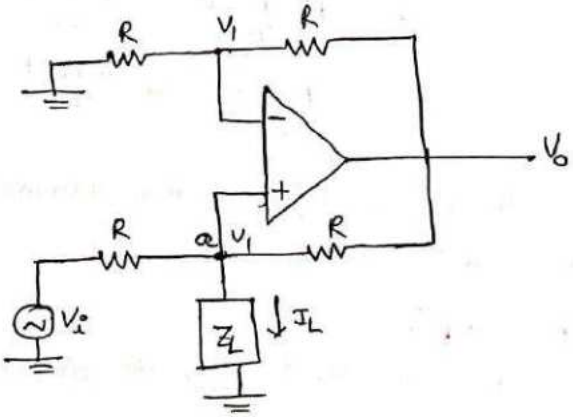
Nodal equation at node 'a', is

$$\left(\frac{V_1 - V_i}{R}\right) + \left(\frac{V_1 - V_o}{R}\right) + I_L = 0$$

$$\frac{V_1 - V_i + V_1 - V_o + I_L R}{R} = 0$$

$$2V_1 - V_i - V_o + I_L R = 0$$

$$2V_1 = V_i + V_o - I_L R \rightarrow (1)$$



Since the op-amp is connected in non-inverting configuration.

$$\therefore \quad V_o = \left(1 + \frac{R}{R}\right) V_1 = 2V_1 \rightarrow (2)$$

Substitute eq(1) in eq(2), we have

$$V_o = V_i + V_o - I_L R \Rightarrow V_i = I_L R$$

$$\boxed{I_L = \frac{V_i}{R}}$$

Input voltage is converted to o/p current I_L.

Current-to-Voltage Converter (Transresistance Amplifier)

Photo cell, photodiode and photo voltaic cell give an o/p current that is proportional to an incident light. The current through these devices can be converted to voltage by using I-V Converter. and thereby the amount of light energy incident on photo device can be measured.

Since (-) i/p terminal is at virtual ground, no current flows through R_s.

writing nodal equation at virtual ground.

$$\left(\frac{0-V_o}{R_f}\right) - I_s = 0$$

$$\therefore \quad \boxed{V_o = -I_s R_f}$$

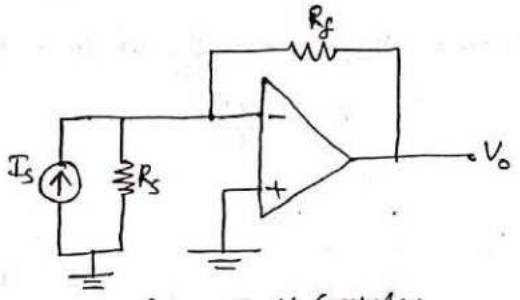
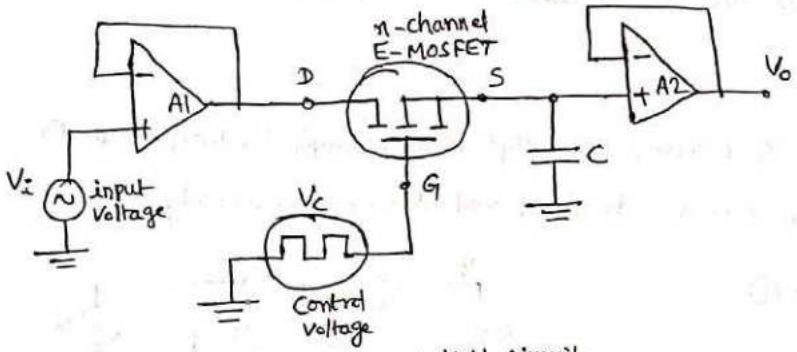


Fig:- I-V Converter

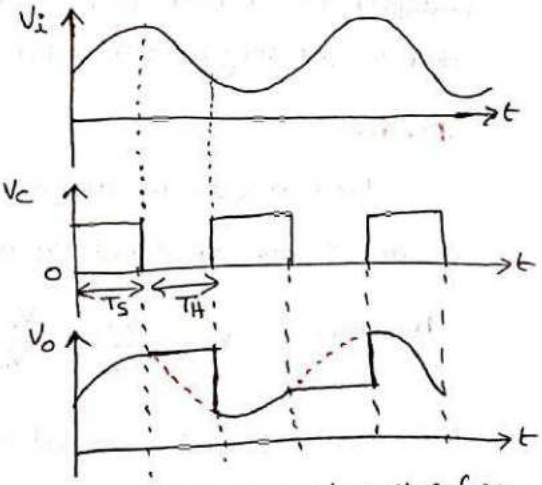
From the above equation, we can say i/p current I_s is converted to o/p voltage V_o.

Sample and Hold Circuit

A sample and Hold circuit samples an i/p signal and holds on to its last sampled value until the i/p signal is sampled again. This circuit is very useful in digital interfacing, analog to digital conversion. practical sample and hold circuit is shown in figure



(a) Sample and Hold circuit



(b) Input and output waveforms

Fig (a) & (b):- Sample & Hold circuit with i/p & o/p waveforms.

→ The n-channel E-MOSFET works as switch and is controlled by the control voltage V_c. op-amps A1 and A2 acts as buffers. The analog signal V_i to be sampled is applied to the drain of E-MOSFET and the control voltage V_c is applied to its gate.

→ When V_c is +ve, E-MOSFET turn on and the capacitor charges to the instantaneous value of input V_i. Thus the i/p voltage V_i appears across the capacitor C and then at the o/p through buffer A2.

→ when V_c is -ve, E-MOSFET is off. The capacitor C is now facing the high i/p impedance of A2. and hence cannot discharge. the capacitor holds the voltage across it. The time period T_H during which ~~V_c is held Cons~~ voltage across the capacitor held constant is called Holding period.

→ Time period T_S during which voltage across capacitor is equal to i/p voltage is called Sampling period.

Multiplier

A basic multiplier symbol is shown in figure. Two signal inputs V_x and V_y are provided.

The output voltage, $\boxed{V_o = \frac{V_x V_y}{V_{ref}}}$

Normally, V_{ref} is internally set to 10 volts.

$\therefore V_o = \frac{V_x V_y}{10}$.

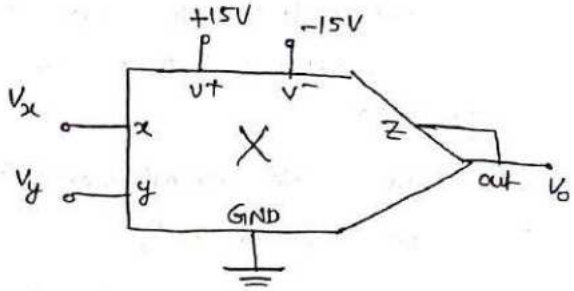


Fig:- Multiplier Schematic symbol.

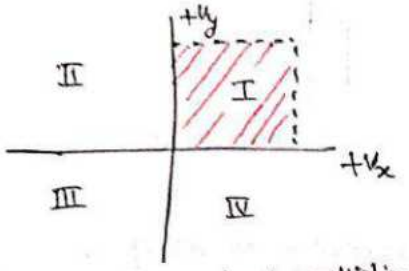
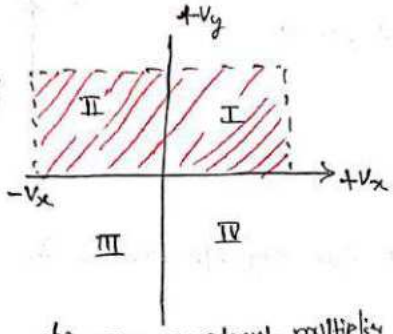
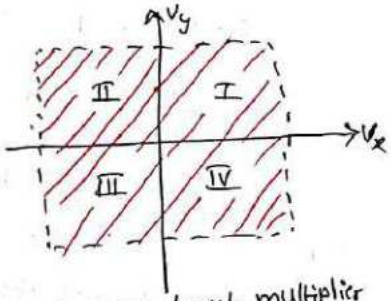


Fig:- (a) one-quadrant multiplier



(b) Two-quadrant multiplier



(c) Four-quadrant multiplier

If both inputs are +ve, the IC is said to be one quadrant multiplier. A two quadrant multiplier will function properly if one i/p is held +ve and the other is allowed to be both +ve or −ve. If both i/ps may be either +ve or −ve, the IC is called a four quadrant multiplier.

Divider

Division can be accomplished by placing the multiplier in op-amp's feedback loop. For divider circuit i/p signals V_z and V_x acts as dividend and divisor respectively.

From figure, $V_A = \frac{V_x V_y}{V_{ref}} = \frac{V_x V_o}{V_{ref}} \rightarrow (1)$

Nodal equation at (−) i/p terminal is

$\left(\frac{0-V_z}{R}\right) + \left(\frac{0-V_A}{R}\right) = 0$:

$-V_z = V_A \rightarrow (2)$

Substitute eq (1) in eq (2), we get

$-V_z = \frac{V_x V_o}{V_{ref}} \Rightarrow \boxed{V_o = -V_{ref}\left(\frac{V_z}{V_x}\right)}$

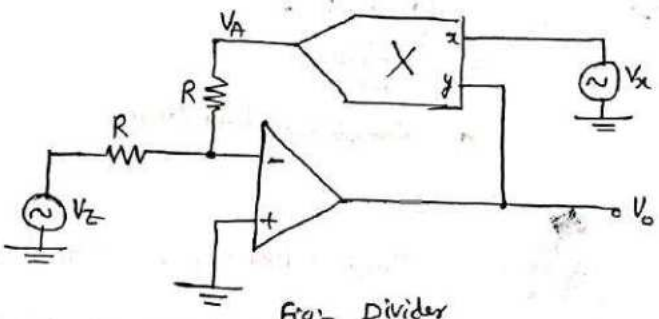


Fig:- Divider

Differentiator

Circuit performs the mathematical operation of differentiation, i.e, the o/p waveform is the derivative of i/p waveform. A Differentiator circuit is shown in figure

Analysis

Node 'a' is at virtual ground.

Nodal equation at node 'a' is.

$\left[C_1 \frac{d(0-V_i)}{dt}\right] + \left(\frac{0-V_o}{R_f}\right) = 0$.

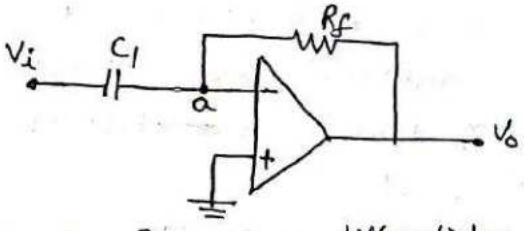


Fig:- op-amp differentiator.

$$-C_1\frac{dV_i}{dt} = \frac{V_o}{R_f} \Rightarrow \boxed{V_o = -R_f C_1 \frac{dV_i}{dt}}$$

Thus the o/p voltage V_o is a constant $(-R_f C_1)$ times the derivative of the i/p voltage V_i. The minus sign indicates a 180° phase shift of the o/p waveform V_o with respect to the i/p signal.

$\Rightarrow$ From figure, $\frac{V_o}{V_i} = -\frac{R_f}{1/j\omega C_1} \Rightarrow A = \frac{V_o}{V_i} = -j\omega C_1 R_f$

$|A| = \omega R_f C_1 = f/f_a$, where $f_a = \frac{1}{2\pi R_f C_1}$

at $f = f_a$, $|A| = 1$ i.e. 0 dB.

(1) As f increases gain also increases and differentiator may become unstable

(2) i/p impedance decreases with frequency, thereby making the ckt sensitive to high frequency noise.

Practical Differentiator

A practical differentiator eliminates the problems of instability and high frequency noise.

$\frac{V_o}{V_i} = -\frac{Z_f}{Z_1}$, where $Z_f = R_F \parallel \frac{1}{j\omega C_F}$

$Z_f = \frac{R_F}{1+j\omega R_F C_F}$ and

$Z_1 = R_1 + \frac{1}{j\omega C_1} = \frac{1+j\omega C_1 R_1}{j\omega C_1}$

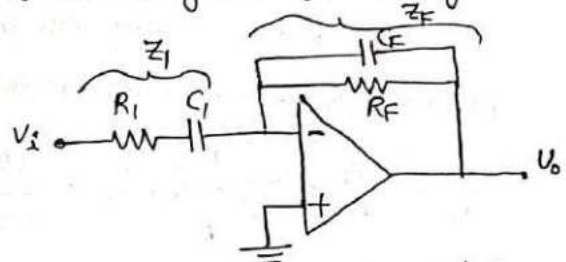


Fig:- practical differentiator

$\therefore A = \frac{V_o}{V_i} = -\frac{j\omega C_1 R_F}{(1+j\omega R_F C_F)(1+j\omega C_1 R_1)}$

For $R_F C_F = R_1 C_1$, we get $A = \frac{V_o}{V_i} = \frac{-j\omega R_F C_1}{(1+j\omega R_1 C_1)^2} = -\frac{j\omega R_F C_1}{(1+j\,f/f_b)^2}$, where $f_b = \frac{1}{2\pi R_1 C_1}$

For $f < f_b$, gain increases

For $f > f_b$, gain decreases. Thus gain at high frequency is reduced thereby avoiding high frequency noise and stability problems.

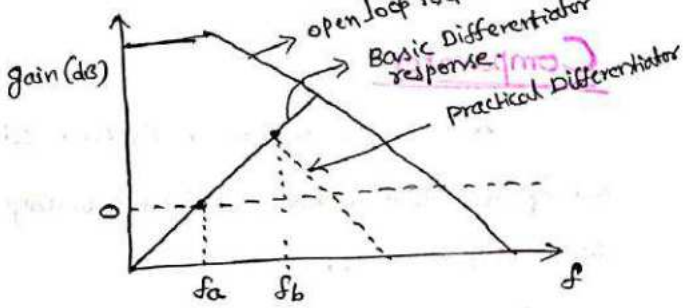


Fig: Frequency Response.

For good differentiation, time period T of the i/p signal is $\boxed{T \geq R_F C_1}$.

Design steps

(1) Choose f_a equal to the highest frequency of the i/p signal. Assume C_1 ($< 1\,\mu f$) and then calculate R_F.

(2) Choose $f_b = 10 f_a$. Now calculate the values of R_1 and C_F so that $R_1 C_1 = R_F C_F$.

Integrator

If we interchange the resistor and capacitor of the differentiator, we get Integrator.

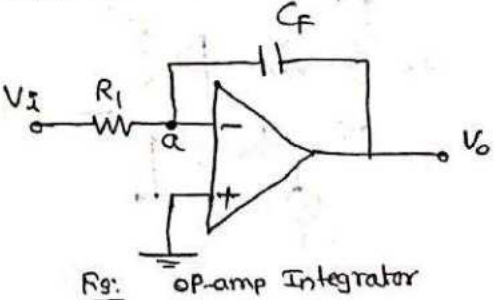


Fig: op-amp Integrator

Nodal equation at node 'a' is

$\left(\frac{0-V_i}{R_1}\right) + C_F\frac{d(0-V_o)}{dt} = 0$

$-\frac{V_i}{R_1} - C_F\frac{dV_o}{dt} = 0 \Rightarrow -\frac{V_i}{R_1} = C_F\frac{dV_o}{dt}$

Integrating on both sides, we get

$$V_o = -\frac{1}{R_1 C_F}\int V_i\, dt$$; output voltage is proportional to the integration of i/p.

$$\Rightarrow \frac{V_o}{V_i} = -\frac{Z_f}{Z_1} = -\frac{1/j\omega C_F}{R_1} = -\frac{1}{j\omega C_F R_1}$$

$$|A| = \left|\frac{V_o}{V_i}\right| = \frac{1}{\omega C_F R_1} = \frac{1}{(f/f_b)}, \quad \text{where } f_b = \frac{1}{2\pi R_1 C_F}$$

at $f = f_b$, $|A| = 1$ i.e. 0 dB.

for $f = 0$, $|A| = \infty$, and op-amp saturates

for $f < f_b$, gain decreases.

Practical Integrator (Lossy Integrator)

gain at low frequency can be limited by placing R_F in parallel to C_F to avoid saturation. problem. R_F limits the low frequency gain and thus provides stabilization.

$$\frac{V_o}{V_i} = -\frac{Z_f}{Z_1} = -\frac{\left(\frac{R_F}{1+j\omega R_F C_F}\right)}{R_1} = -\frac{(R_F/R_1)}{1+j\omega R_F C_F}$$

$$A = \frac{V_o}{V_i} = \frac{-(R_F/R_1)}{1+j\,f/f_a}, \quad \text{where } f_a = \frac{1}{2\pi R_F C_F}$$

For $f = 0$, $A = -\frac{R_F}{R_1}$

For $f > f_a$, gain decreases

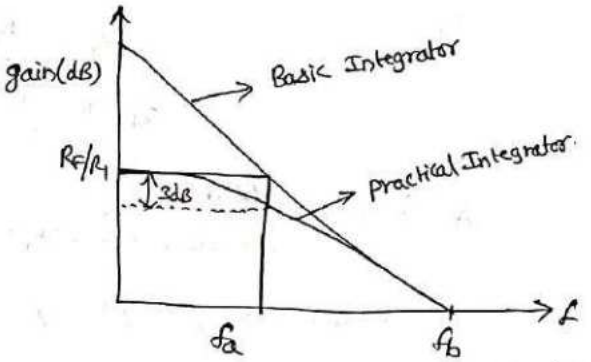


Fig:- Frequency response of Lossy Integrator

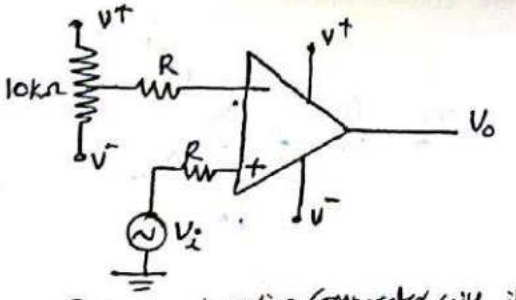
For good Integration, time period T of the i/p signal is $T \geq R_F C_F$.

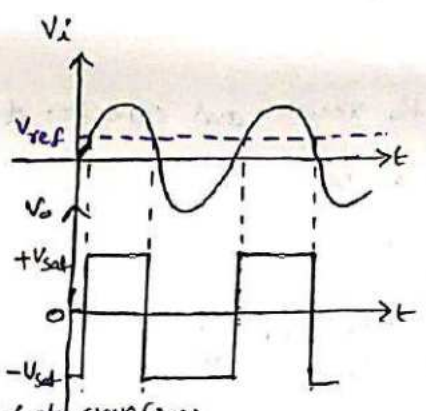
Comparator

A Comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. It is basically an open loop op-amp with output $\pm V_{sat}$.

There are basically two types of Comparators (i) Non-inverting Comparator
(ii) Inverting Comparator.

(i) Non-inverting Comparator





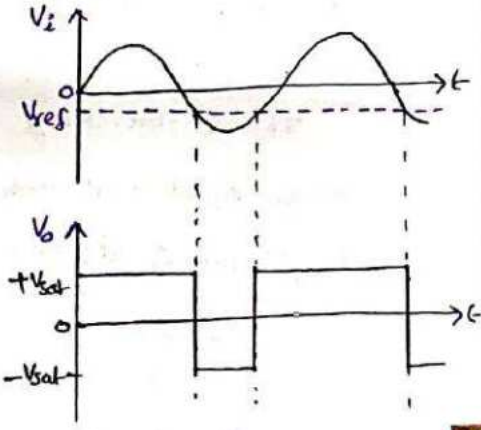


Fig:- Non-inverting Comparator with i/p & o/p waveforms

A fixed reference voltage V_{ref} is applied to -ve i/p and a varying signal V_i is applied to (+) i/p. when $V_i > V_{ref}$, output voltage, $V_o = +V_{sat}$

when $V_i < V_{ref}$, output voltage, $V_o = -V_{sat}$.

→ input and output waveforms for two different reference voltages are shown in figure.

(ii) Inverting Comparator

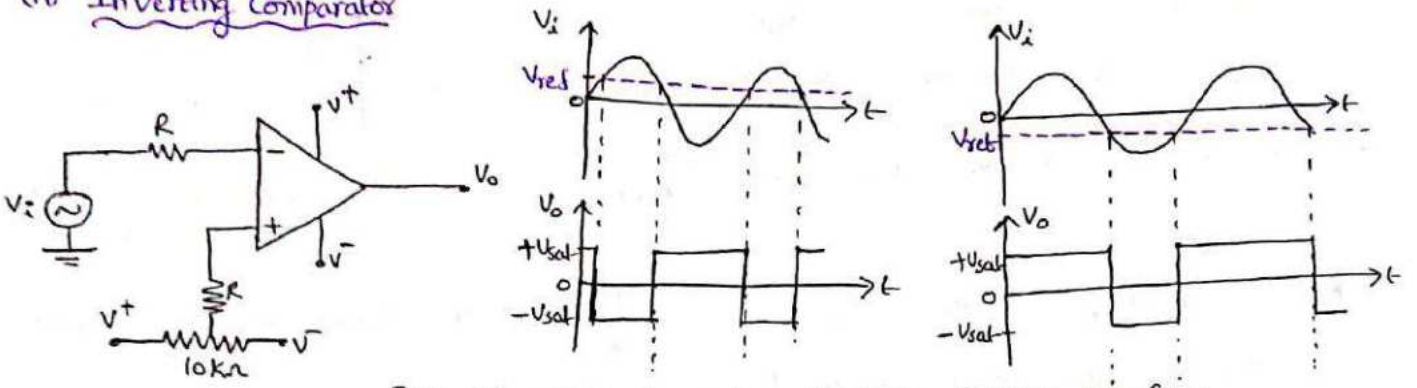


Fig:- Inverting Comparator with input and output waveforms.

⇒ i/p signal V_i applied to (-) i/p and reference voltage, V_{ref} is applied to (+) i/p through 10kΩ potentiometer. when $V_i > V_{ref}$, output voltage, $V_o = -V_{sat}$

when $V_i < V_{ref}$, output voltage, $V_o = +V_{sat}$

⇒ Figure shows i/p and o/p waveforms for different reference voltages are shown in figure.

Regenerative Comparator (Schmitt-Trigger)

Figure shows the inverting comparator with +ve feedback. This circuit convert irregular shaped waveforms to a square wave.

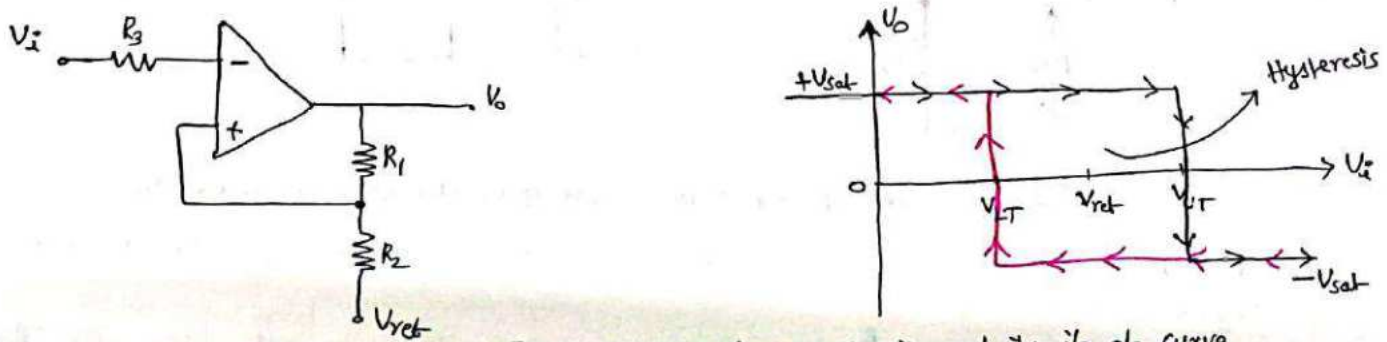


Fig:- Schmitter trigger circuit and its i/p-o/p curve.

→ The i/p voltage is applied to the (-) i/p terminal and feedback voltage to the (+) i/p terminal. The i/p voltage V_i triggers the o/p V_o every time it exceeds certain voltage levels. These voltage levels are called upper threshold voltage (V_{UT}) and lower threshold voltage (V_{LT}). The hysteresis width is the difference between these two threshold voltages.

→ When $V_o = +V_{sat}$

Voltage at (+) i/p terminal is obtained by using superposition

$$V_{UT} = \frac{V_{ref} R_1}{R_1 + R_2} + \frac{R_2 V_{sat}}{R_1 + R_2}$$

When $V_i < V_{UT}$, the output $V_o = +V_{sat}$.

When $V_i > V_{UT}$, the o/p V_o switches from $+V_{sat}$ to $-V_{sat}$.

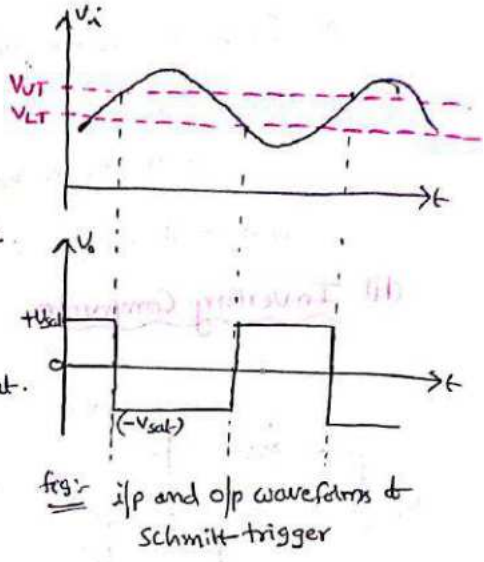


fig:- i/p and o/p waveforms of schmitt-trigger

When $V_o = -V_{sat}$

Voltage at (+) i/p terminal is $V_{LT} = \frac{V_{ref} R_1}{R_1+R_2} - \frac{R_2 V_{sat}}{R_1+R_2}$

when $V_i > V_{LT}$, the o/p $V_o = -V_{sat}$

When $V_i < V_{LT}$, the o/p V_o switches from $-V_{sat}$ to $+V_{sat}$.

$\Rightarrow$ Hysteresis width, $V_H = V_{UT} - V_{LT} = \frac{2R_2 V_{sat}}{R_1+R_2}$.

Note:- If $V_{ref} = 0$ V, then $V_{UT} = -V_{LT} = \frac{R_2 V_{sat}}{R_1+R_2}$. If a sinusoidal voltage is applied to this comparator, we get symmetrical square wave output.

Square wave Generator (Astable Multivibrator)

A simple op-amp square wave generator is shown in figure. It is also called a free running oscillator.

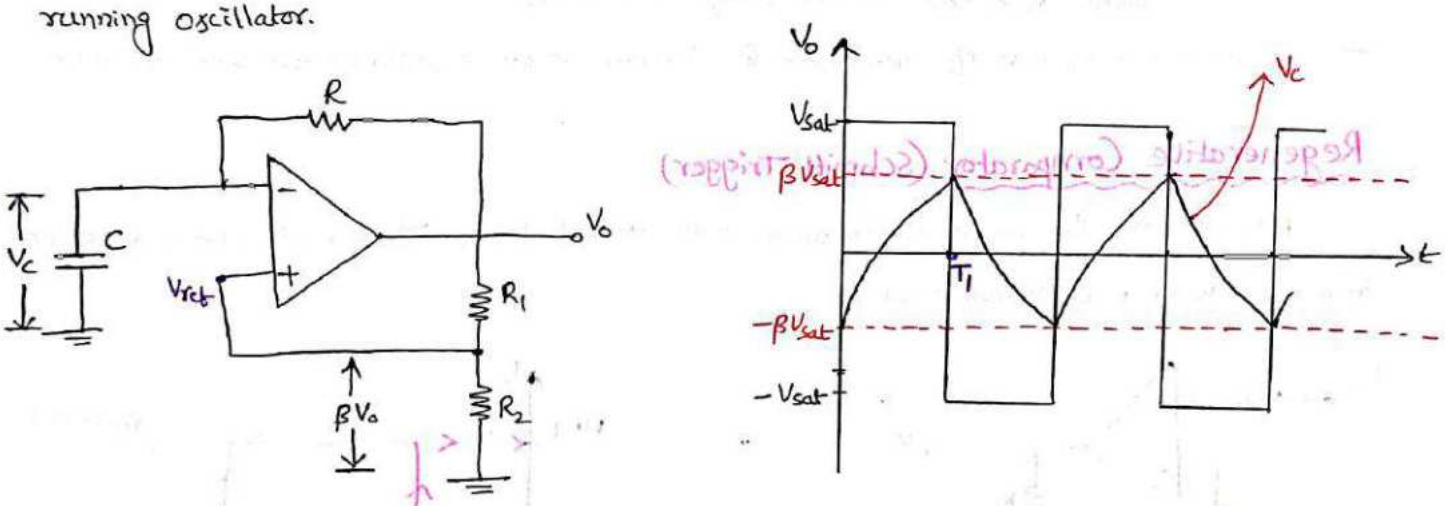


Fig:- Simple op-amp square wave generator with its waveform

→ Principle of generation of square wave output is to force an op-amp to operate in saturation region.

→ Fraction of output $\beta = \frac{R_2}{R_1+R_2}$ is fedback to the (+) i/p terminal. Thus $V_{ref} = \beta V_o$. The output is also fedback to the (−) i/p through lowpass RC combination.

→ Whenever i/p at (−) i/p terminal just exceeds the V_{ref} switching takes place resulting in a square wave output. In Astable Multivibrator both the states are quasi stable.

Operation

$\Rightarrow$ When $V_o = +V_{sat}$, capacitor C charging towards $+V_{sat}$ through R. Now voltage at (+) i/p terminal is $+\beta V_{sat}$. As the voltage across the capacitor, V_c just exceeds βV_{sat}, output is switches to $-V_{sat}$.

⇒ Now Capacitor discharges through R, i.e, it is charging towards $-V_{sat}$. As the capacitor voltage just exceeds $-\beta V_{sat}$, output switches back to $+V_{sat}$. The cycle repeat itself and square wave is generated at the output.

Output Frequency

Frequency is determined by the time it takes the capacitor to charge from $-\beta V_{sat}$ to $+\beta V_{sat}$ and vice-versa.

The voltage across the capacitor as a function of time, $V_c(t) = V_f + (V_i - V_f)e^{-t/RC}$.

From the figure, $V_f = +V_{sat}$ and $V_i = -\beta V_{sat}$

$$\therefore V_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat})e^{-t/RC} = V_{sat} - V_{sat}(1+\beta)e^{-t/RC}$$

At $t = T_1$, $V_c(t) = \beta V_{sat}$. Therefore above equation becomes

$$\beta V_{sat} = V_{sat} - V_{sat}(1+\beta)e^{-T_1/RC}$$

$$\beta V_{sat} = V_{sat}\left[1 - (1+\beta)e^{-T_1/RC}\right] \Rightarrow e^{-\frac{T_1}{RC}} = \frac{1-\beta}{1+\beta}$$

$$e^{\frac{T_1}{RC}} = \frac{1+\beta}{1-\beta}$$

$$\therefore T_1 = RC\ln\left(\frac{1+\beta}{1-\beta}\right) \text{ ; This is one-half of the period.}$$

$$\therefore \text{Total time period, } \boxed{T = 2T_1 = 2RC\ln\left(\frac{1+\beta}{1-\beta}\right)} \text{ ;}$$

→ If $R_1 = R_2$, then $\beta = 0.5$ and $T = 2RC\ln(3)$

if $R_1 = 1.16R_2$, $T = 2RC$ and $f_0 = \frac{1}{2RC}$

⇒ In the waveform, the o/p swings from $+V_{sat}$ to $-V_{sat}$. So the total peak to peak output voltage $= 2V_{sat}$.

Monostable Multivibrator

→ Monostable Multivibrator has one stable state and other is quasi stable state.

→ Circuit is useful for generating o/p pulse of adjustable time duration in response to a triggering signal.

→ The width of the pulse depends on the External Components Connected to the op-amp.

→ Diode D_1 clamps the capacitor voltage to $V_D = 0.7V$ when the o/p is $+V_{sat}$.

→ A -Ve trigger pulse is applied to the +Ve terminal through R_4-C_4 and D_2 combination.

Operation

(a) Let us assume that circuit is in stable state i.e, $V_0 = +V_{sat}$.

Diode D_1 conducts and voltage across the capacitor is clamped to 0.7V and the voltage at (+) i/p terminal is $+\beta V_{sat}$.

Voltage at (+) i/p is always greater than (−) i/p terminal, Thus o/p is $V_0 = +V_{sat}$. The output remains in same state. Hence it is stable state.

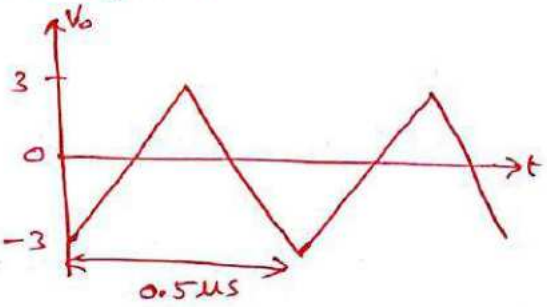
(5) A non-inverting amplifier with a gain of 100 is nulled at 25°C. what will happen to the o/p voltage if the temperature rises to 50°C for an offset voltage drift of 0.15 mV/°C ?

Sol:- Input offset voltage due to temperature rise $= 0.15 \times 10^{-3} (50-25) = 3.75$ mV.

o/p voltage, $V_o = A_{CL} \cdot V_{io}$

$= 100 \times 3.75 \times 10^{-3} = \underline{375 \text{ mV}}$

(6) The o/p of an op-amp voltage follower is a triangular wave shown in figure. what is the slew rate of op-amp?



Sol:- Slew rate is the maximum rate of change of the output.

$\therefore SR = \frac{6}{\left(\frac{0.5}{2}\right) \times 10^{-6}} = 14 \frac{V}{\mu s}$.

(7) A 741C op-amp is used as an inverting amplifier with a gain of 50. The voltage gain vs frequency curve is Flat upto 20KHz. what maximum peak to peak ~~voltage~~ input signal can be applied without distorting the output?

Sol:- Given that, gain = 50, $f = 20$KHz.

For 741C op-amp, Slew rate, $SR = 0.5$ V/μs.

$$SR = \frac{2\pi f V_m}{10^6} \text{ V/μs}$$

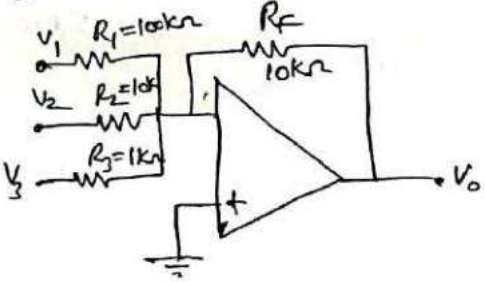
$$0.5 = \frac{2\pi \times 20 \times 10^3 \times V_m}{10^6} \Rightarrow \underline{V_m = 3.98 \text{ V Peak.}}$$

So. $V_o = 2V_m = 7.96$ V

we know gain $= \frac{V_o}{V_i} \Rightarrow V_i = \frac{V_o}{\text{gain}} = \frac{7.96}{50} = \underline{159 \text{ mV}}$

(8) Design an adder circuit using an op-amp to get the o/p expression as $V_o = -(0.1V_1 + V_2 + 10V_3)$. where V_1, V_2 and V_3 are the inputs.

Sol:- from the given expression, we can say that circuit is inverting Summing Amplifier with o/p, $V_o = -\left[\frac{R_F}{R_1} V_1 + \frac{R_F}{R_2} V_2 + \frac{R_F}{R_3} V_3\right] \rightarrow (1)$



by comparing eq(1) with given V_o, we can write.

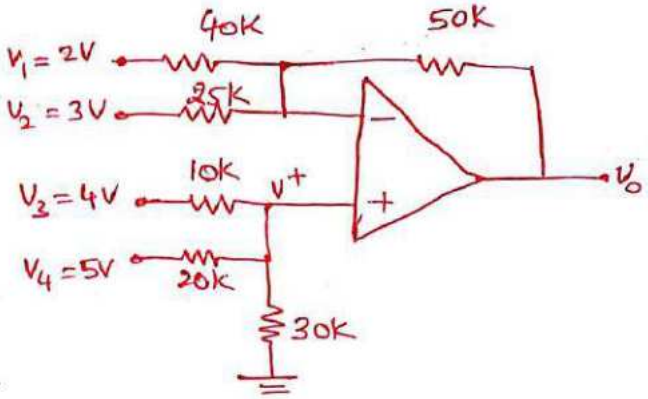
$\frac{R_F}{R_1} = 0.1$, $\frac{R_F}{R_2} = 1$, $\frac{R_F}{R_3} = 10$

Let $R_F = 10$KΩ, then $R_1 = \frac{R_F}{0.1} = \frac{10K}{0.1} = 100$KΩ

$R_2 = R_F = 10$KΩ

$R_3 = \frac{R_F}{10} = \frac{10K}{10} = 1$KΩ

(9) Find V_o for the adder Subtractor shown in figure.



Sol:- o/p due to V_1 only

$$V_{o1} = -\frac{50K}{40K} \times 2 = -2.5V$$

o/p due to V_2 only

$$V_{o2} = -\frac{50K}{25K} \times 3 = -6\ V$$

o/p due to V_3 only

$R_F = 50K$, $R_1 = 40K \| 25K = 15.385K\Omega$

$$V^+ = 4 \times \frac{(20\|30)}{(20\|30)+10K} = 2.18\ V$$

$$V_{o3} = \left(1+\frac{R_F}{R_1}\right) V^+ = \left(1+\frac{50K}{15.385K}\right)(2.18) = 9.27V$$

o/p due to V_4 only

$R_F = 50K$, $R_1 = 40K \| 25K = 15.385K\Omega$

$$V^+ = \frac{(10\|30)}{(10\|30)+20} \times 5 = 1.364\ V$$

$$V_{o4} = \left(1+\frac{R_F}{R_1}\right) V^+ = \left(1+\frac{50K}{15.385K}\right)(1.364) = 5.80\ V$$

from Superposition theorem, total o/p voltage, $V_o = V_{o1}+V_{o2}+V_{o3}+V_{o4}$

$$= (-2.5)+(-6)+9.27+5.80$$

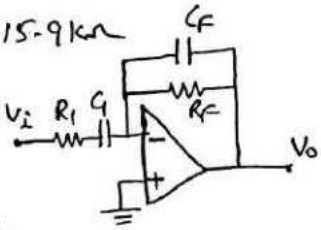
$$V_o = 6.57\ V$$

(10) (i) Design an op-amp differentiator that will differentiate an i/p signal with $f_{max} = 100\ Hz$

(ii) Draw the o/p waveform for a sinewave of 1V peak at 100Hz applied to the differentiator

Sol:- (a) Select $f_a = f_{max} = 100\ Hz = \frac{1}{2\pi R_F C_1}$

Let $C_1 = 0.1\mu F$, then $R_F = \frac{1}{2\pi C_1 f_a} = \frac{1}{2\pi \times 0.1\times10^{-6}\times100} = 15.9K\Omega$



$$f_b = 10 f_a = 10\times100 = 1KHz = \frac{1}{2\pi R_1 C_1}$$

$$\therefore R_1 = \frac{1}{2\pi C_1 f_b} = \frac{1}{2\pi\times0.1\times10^{-6}\times1000} = 1.59K\Omega$$

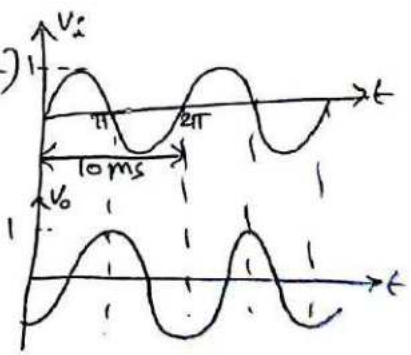
Since $R_F C_F = R_1 C_1 \Rightarrow C_F = \frac{R_1 C_1}{R_F} = \frac{1.59\times10^3\times0.1\times10^{-6}}{15.9\times10^3} = 0.01\mu F$

(b) $V_i = 1 \sin 2\pi 100t$

$$V_o = -R_F C_1 \frac{dV_i}{dt} = -(15.9\times10^3)(0.1\times10^{-6})\frac{d}{dt}(1\sin 2\pi 100t)$$

$$= -(15.9\times10^3)(0.1\times10^{-6})(2\pi\times100)\cos 2\pi 100t$$

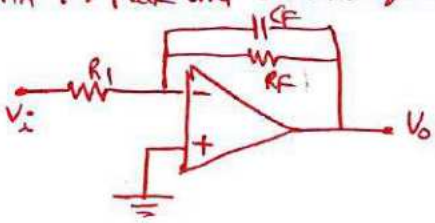
$$= -0.999\cos 2\pi 100t$$



(11) For the Lossy Integrator shown in figure. with $R_1 = 10k\Omega$, $R_F = 100k\Omega$, $C_F = 10nF$.

(a) Determine the lower frequency limit of Integration

(b) Draw the response for the input a Sinusoidal signal with 1'V peak and 5 KHz frequency



Sol:-

(a) Lower frequency limit of integration = f_a

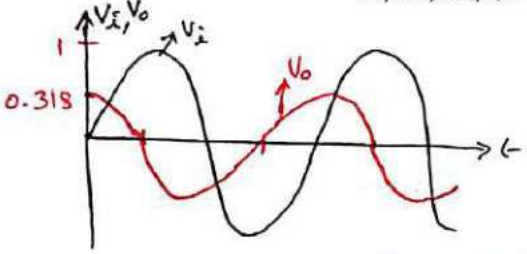
$$f_a = \frac{1}{2\pi R_F C_F} = \frac{1}{2\pi \times 100 \times 10^3 \times 100 \times 10^{-9}}$$

$$= 159 \text{ Hz}.$$

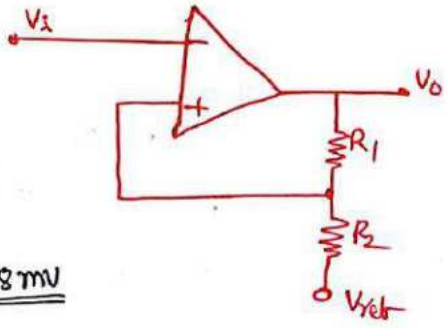
(b) $V_m = 1V$, $f = 5$ KHz, $\therefore V_i = 1 \sin 2\pi 5000t$.

for integrator, $V_o(t) = -\frac{1}{R_1 C_F}\int V_i\, dt = -\frac{1}{10\times10^3 \times 10\times10^{-9}} \int \sin(2\pi 5000t)\, dt$

$$V_o(t) = -\frac{1}{10\times10^3\times10\times10^{-9}} \left[\frac{-\cos(2\pi 5000t)}{2\pi \times 5000}\right] = \underline{0.318 \cos(2\pi 5000t)}$$



(12) For the Schmitt Trigger shown in figure, $R_2 = 100\Omega$, $R_1 = 50k\Omega$, $V_{ref} = 0V$, $V_i = 1 V_{pp}$. Sine wave and Saturation Voltage = $\pm 14V$. Determine threshold voltages V_{UT} and V_{LT}.



Sol:- V_{UT} and V_{LT} are voltages at (+) i/p terminal when $V_o = +V_{sat}$ and $V_o = -V_{sat}$ respectively.

$$\therefore V_{UT} = \left(\frac{R_2}{R_1+R_2}\right)(V_{sat}) = \left(\frac{100}{50\times10^3+100}\right)(14) = \underline{28mV}$$

$$V_{LT} = \left(\frac{R_2}{R_1+R_2}\right)(-V_{sat}) = \left(\frac{100}{50\times10^3+100}\right)(-14) = \underline{-28mV}$$

UNIT - III

Filter:

An electronic filter is a frequency selective circuit that passes specified band of frequencies and blocks or attenuates signal's of frequencies outside the band.

Pass band :- The range of frequencies which are allowed to pass through the filter is called pass band

Stop band :- The range of frequencies which are not allowed (rejected) by the filter is called stop band.

→ Filters may be classified as (1) Analog or Digital Filters
(2) Active or passive Filters
(3) Audio or Radio frequency Filters

Active Filters

Active Filters uses op-amp as active element along with Resistors and Capacitors.

Advantages of Active Filters over passive Filters

① Gain and frequency adjustment Flexibility

Since the op-amp is capable of providing gain, the input signal is not attenuated as in a passive filter. Active Filters are easier to tune and adjust.

② No Loading problem

Because of the high input resistance and low output resistance of the op-amp, the active filter does not cause loading of the source or load.

③ Cost

Active Filters are more economical than passive Filters.

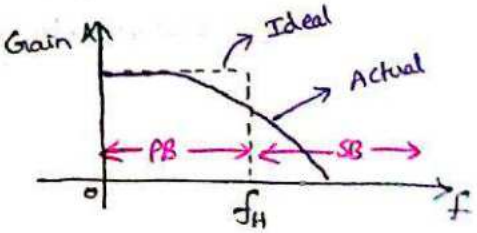
Applications of Active Filters

① In Communication & Signal processing
② Radio, Television
③ Radar, Satellites
④ Bio-medical equipment.

⇒ The most commonly used Filters are
① Low pass Filter (LPF)
② High pass Filter (HPF)
③ Band pass Filter (BPF)
④ Band Reject Filter (BRF)
⑤ All pass Filter.

Low pass Filter

A Low pass Filter passes all the low frequencies upto cut-off frequency and rejects or attenuates the frequencies above cut-off frequency (f_H).



First order LowPass Filter

1st order LPF uses RC network for filtering. OP-amp is used in non-inverting configuration. Resistors R_1 and R_F determine the gain of the Filter.

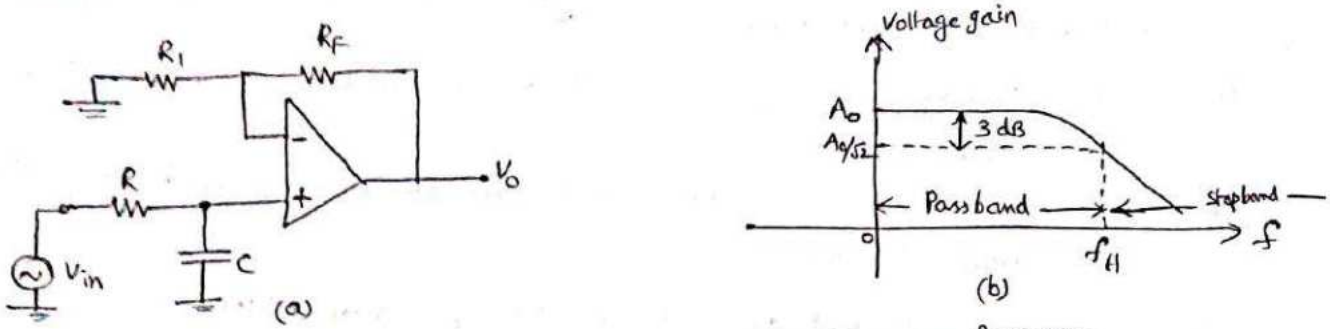


Fig: (a) First order LPF (b) Frequency Response.

Voltage V_1 across the capacitor is, $V_1 = \frac{(1/j\omega C)}{R + \frac{1}{j\omega C}} V_{in} = \left(\frac{1}{1+j\omega RC}\right) V_{in}$

The output voltage, $V_o = \left(1 + \frac{R_F}{R_1}\right) V_1$

$$V_o = \left(1 + \frac{R_F}{R_1}\right) \frac{1}{1+j\omega RC} V_{in} \Rightarrow \boxed{\frac{V_o}{V_{in}} = \frac{A_o}{1+j\omega RC}}, \text{ where } A_o = 1 + \frac{R_F}{R_1}$$

$$\frac{V_o}{V_{in}} = \frac{A_o}{1+j2\pi fRC} = \frac{A_o}{1+j f/f_H}, \text{ where } \boxed{f_H = \frac{1}{2\pi RC}}$$

Magnitude and Phase of voltage gain can be written as

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_o}{\sqrt{1+\left(\frac{f}{f_H}\right)^2}}$$

where A_o = Passband gain
f_H = cutoff frequency
f = frequency of the input signal.

$$\phi = -\tan^{-1}\left(\frac{f}{f_H}\right)$$

→ At very low frequencies i.e, $f < f_H$, $\left|\frac{V_o}{V_{in}}\right| \cong A_o$

at $f = f_H$, $\left|\frac{V_o}{V_{in}}\right| = \frac{A_o}{\sqrt{2}}$

at $f > f_H$, $\left|\frac{V_o}{V_{in}}\right| << A_o \cong 0$.

Thus the LPF has a constant gain A_o from 0 Hz to the high cutoff frequency f_H. At f_H the gain is $A_o/\sqrt{2}$, and after f_H gain decreases at a constant rate.

Filter Design

Steps

1. Choose the value of High cutoff frequency f_H
2. Select a value of $C \leq 1\mu F$.
3. Calculate the value of R using

$$\boxed{R = \frac{1}{2\pi f_H C}}$$

Second order Active Filter

Filter response can be improved by using a 2nd order active Filters.

⇒ If we use higher order Filters, filter response will become more and more closer to the ideal Filter response.

→ op-amp is connected as non-inverting amplifier

$$V_o = \left(1+\frac{R_F}{R_1}\right) V_B = A_o V_B \rightarrow (1)$$

$$A_o = 1+\frac{R_F}{R_1} \rightarrow (2)$$

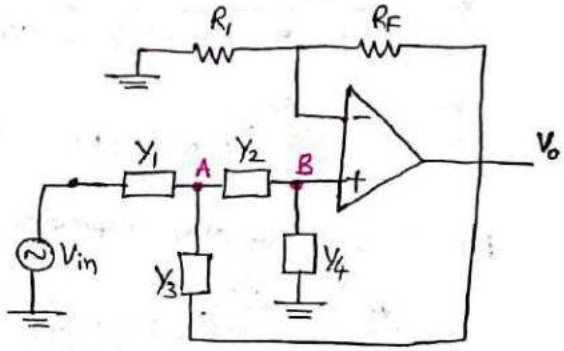


Fig:- 2^n order General purpose Filter

at node A

$$(V_A - V_{in})Y_1 + (V_A - V_B)Y_2 + (V_A - V_o)Y_3 = 0$$

$$V_A(Y_1+Y_2+Y_3) - V_o Y_3 - V_B Y_2 - V_{in} Y_1 = 0$$

$$V_A(Y_1+Y_2+Y_3) - V_o Y_3 - V_B Y_2 = V_{in} Y_1 \rightarrow (3)$$

at Node-B

$$(V_B - V_A)Y_2 + V_B Y_4 = 0$$

$$V_B(Y_2+Y_4) - V_A Y_2 = 0 \Rightarrow V_B(Y_2+Y_4) = V_A Y_2 \rightarrow (4)$$

$$\frac{V_o}{A_o}(Y_2+Y_4) = V_A Y_2 \Rightarrow V_A = \frac{V_o}{A_o}\left(\frac{Y_2+Y_4}{Y_2}\right) \rightarrow (5)$$

Substitute equation (5), (1) into equation (3), we get

$$\frac{V_o}{A_o}\left(\frac{Y_2+Y_4}{Y_2}\right)(Y_1+Y_2+Y_3) - V_o Y_3 - \frac{V_o}{A_o} Y_2 = V_{in} Y_1$$

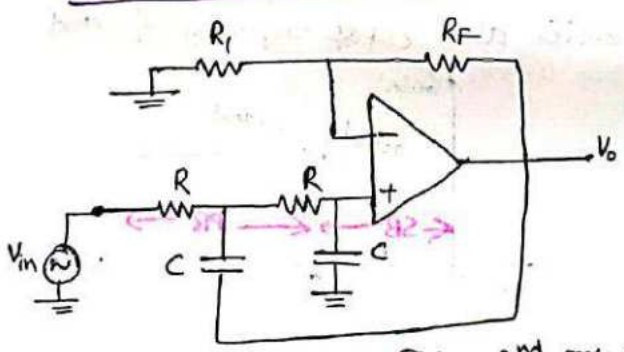
$$\frac{V_o}{A_o}\left[\frac{(Y_2+Y_4)(Y_1+Y_2+Y_3)}{Y_2} - A_o Y_3 - Y_2\right] = V_{in} Y_1$$

$$\frac{V_o}{A_o}\left[\frac{Y_1Y_2 + Y_2^2 + Y_2Y_3 + Y_1Y_4 + Y_2Y_4 + Y_3Y_4 - A_oY_2Y_3 - Y_2^2}{Y_2}\right] = V_{in} Y_1$$

$$\boxed{\frac{V_o}{V_{in}} = \frac{A_o Y_1 Y_2}{Y_1Y_2 + Y_4(Y_1+Y_2+Y_3) + Y_2Y_3(1-A_o)}}$$

∴ General purpose voltage gain Expression for 2nd order filter.

Second order Low pass Filter



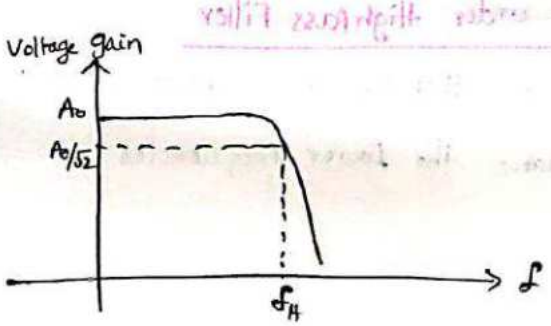


Fig:- 2nd order LPF and its frequency response.

By Comparing with general 2nd order Filter, $Y_1 = Y_2 = \frac{1}{R}$, $Y_3 = Y_4 = SC$.

Substitute above in $\frac{V_o}{V_{in}} = \frac{A_o Y_1 Y_2}{Y_1Y_2 + Y_4(Y_1+Y_2+Y_3) + Y_2Y_3(1-A_o)}$, we get

$$\frac{V_o}{V_{in}} = \frac{A_o \cdot 1/R^2}{\frac{1}{R^2} + sC\left[\frac{1}{R} + \frac{1}{R} + sC\right] + \frac{1}{R} \cdot sC(1-A_o)} = \frac{A_o\, 1/R^2}{\frac{1}{R^2} + sC\left(\frac{2}{R} + sC\right) + \frac{sC}{R}(1-A_o)}$$

Multiply both Numerator and denominator with R^2 we can write

$$\frac{V_o}{V_{in}} = \frac{A_o}{1 + 2sCR + s^2C^2R^2 + sCR - A_o sCR} = \frac{A_o}{s^2C^2R^2 + sCR(3-A_o) + 1}$$

$$\frac{V_o}{V_{in}} = \frac{A_o}{\left(\frac{s}{\omega_h}\right)^2 + \alpha\left(\frac{s}{\omega_h}\right) + 1}$$, where $\omega_h = \frac{1}{RC}$ = Higher cut-off frequency

$\alpha = 3 - A_o$ = Damping coefficient

Put $s = j\omega$ in the above Expression, we get

$$\frac{V_o}{V_{in}} = \frac{A_o}{-\left(\frac{\omega}{\omega_h}\right)^2 + j\alpha\left(\frac{\omega}{\omega_h}\right) + 1} = \frac{A_o}{1 - \left(\frac{\omega}{\omega_h}\right)^2 + j\alpha\left(\frac{\omega}{\omega_h}\right)}$$

$$\boxed{\left|\frac{V_o}{V_{in}}\right| = \frac{A_o}{\sqrt{\left[1 - \left(\frac{\omega}{\omega_h}\right)^2\right]^2 + \left(\alpha\frac{\omega}{\omega_h}\right)^2}}}$$

For 2nd order LPF Flat passband occurs for $\alpha = \sqrt{2}$.

$$\therefore \frac{V_o}{V_{in}} = \frac{A_o}{\left[1 + \left(\frac{\omega}{\omega_h}\right)^4 - 2\left(\frac{\omega}{\omega_h}\right)^2\right] + \left[2\left(\frac{\omega}{\omega_h}\right)^2\right]} \Rightarrow \boxed{\frac{V_o}{V_{in}} = \frac{A_o}{\sqrt{1 + \left(\frac{\omega}{\omega_h}\right)^4}}}$$

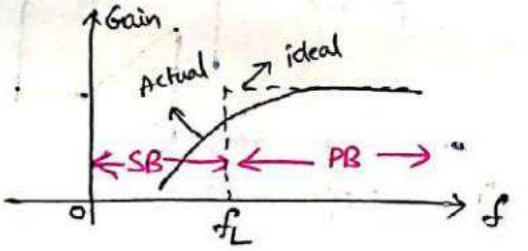
Note:- For nth order Filter, $\boxed{\frac{V_o}{V_{in}} = \frac{A_o}{\sqrt{1 + \left(\frac{\omega}{\omega_h}\right)^{2n}}}}$

Note:- To Design higher order Filters use the following denominator Polynomials

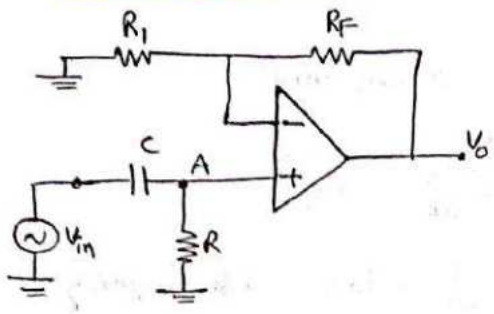
order	Polynomials
1	$s+1$
2	$(s^2 + 1.414s + 1)$
3	$(s+1)(s^2+s+1)$
4	$(s^2+0.765s+1)(s^2+1.848s+1)$
5	$(s+1)(s^2+0.618s+1)(s^2+1.618s+1)$

~~First order~~ High Pass Filter

A High Pass Filter Passes all the frequencies above cut-off frequency, f_L and attenuates the lower frequencies.



1st order High Pass Filter



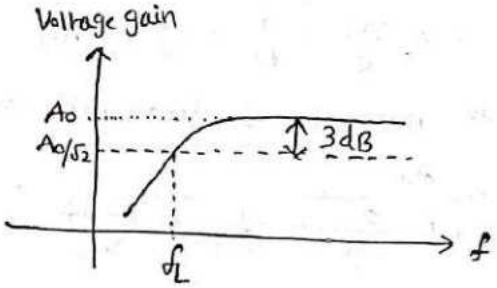


Fig:- 1st order HPF and its frequency response

→ 1st order HPF is formed by interchanging R and C in 1st order LPF. All the frequencies Higher than f_L are passed.

By using voltage division rule, Voltage at node 'A' is

$$V_A = \frac{R}{R+1/j\omega C} V_{in} = \left(\frac{j\omega RC}{1+j\omega RC}\right) V_{in} \rightarrow (1)$$

output voltage, $V_o = \left(1+\frac{R_F}{R_1}\right) V_A$

$$V_o = \left(1+\frac{R_F}{R_1}\right)\left(\frac{j\omega RC}{1+j\omega RC}\right) V_{in}$$

$$\frac{V_o}{V_{in}} = A_o \frac{j2\pi fRC}{1+j2\pi fRC} = \frac{A_o \cdot j(f/f_L)}{1+jf/f_L}$$

where $A_o = 1+\frac{R_F}{R_1}$ = Passband gain

$f_L = \frac{1}{2\pi RC}$ = Lower cut-off frequency

f = freq of i/p signal.

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_o (f/f_L)}{\sqrt{1+(f/f_L)^2}}, \quad \phi = -\tan^{-1} f/f_L + \frac{\pi}{2}$$

Band Pass Filter

→ At very low frequency, $f << f_L$, $\left|\frac{V_o}{V_{in}}\right| < A_o$

at $f = f_L$, $\left|\frac{V_o}{V_{in}}\right| = \frac{A_o}{\sqrt{2}}$

at $f > f_L$, $\left|\frac{V_o}{V_{in}}\right| \cong A_o$.

Second order High pass Filters

High pass Filter is a Complement of LPF and it Can be obtained by interchanging 'R' and 'C' in the LPF.

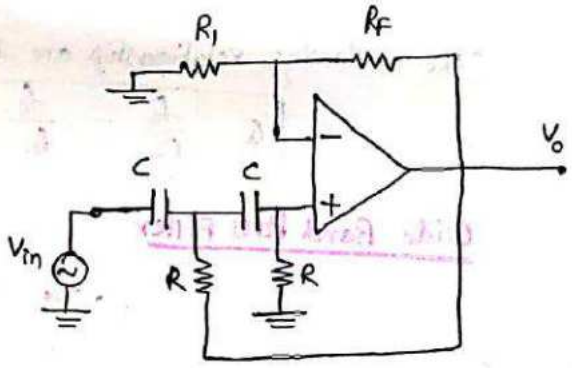


Fig:- 2nd order HPF

for general 2nd order Filter.

$$\frac{V_o}{V_{in}} = \frac{A_o Y_1 Y_2}{Y_1Y_2 + Y_4(Y_1+Y_2+Y_3) + Y_2Y_3(1-A_o)} \rightarrow (1)$$

From the figure, $Y_1 = Y_2 = sC$ and $Y_3 = Y_4 = \frac{1}{R}$.

Substitute Y_1, Y_2, Y_3 and Y_4 in eq (1), we can write

$$\frac{V_o}{V_{in}} = \frac{A_o s^2C^2}{s^2C^2 + \frac{1}{R}(sC+sC+\frac{1}{R}) + sC\cdot\frac{1}{R}(1-A_o)}$$

$$\frac{V_o}{V_{in}} = \frac{A_o s^2 C^2}{s^2C^2 + \frac{2sC}{R} + \frac{1}{R^2} + \frac{sC}{R}(1-A_o)}$$

Divide both numerator & denominator with s^2C^2, we can write.

$$\frac{V_o}{V_{in}} = \frac{A_o}{1 + \frac{2}{sCR} + \frac{1}{s^2C^2R^2} + \frac{(1-A_o)}{sCR}} = \frac{A_o}{1 + \frac{(3-A_o)}{sCR} + \frac{1}{s^2C^2R^2}}$$

$$\frac{V_o}{V_{in}} = \frac{A_o}{1 + \alpha\left(\frac{\omega_l}{s}\right) + \left(\frac{\omega_l}{s}\right)^2}, \quad \text{where, } \omega_l = \frac{1}{RC} = \text{lower cutoff frequency}$$

$$\alpha = 3 - A_o = \text{Damping coefficient}$$

Put $s = j\omega$ in above Expression, we can write

$$\frac{V_o}{V_{in}} = \frac{A_o}{1 - j\alpha\left(\frac{\omega_l}{\omega}\right) - \left(\frac{\omega_l}{\omega}\right)^2} = \frac{A_o}{1 - \left(\frac{\omega_l}{\omega}\right)^2 - j\alpha\left(\frac{\omega_l}{\omega}\right)}$$

$$\boxed{\left|\frac{V_o}{V_{in}}\right| = \frac{A_o}{\sqrt{\left[1 - \left(\frac{\omega_l}{\omega}\right)^2\right]^2 + \left(\alpha\frac{\omega_l}{\omega}\right)^2}}}$$

Flat pass band occurs for $\alpha = \sqrt{2}$,

$$\therefore \left|\frac{V_o}{V_{in}}\right| = \frac{A_o}{\sqrt{1 + \left(\frac{\omega_l}{\omega}\right)^4}}$$

Note:- for nth order HPF, $\left|\frac{V_o}{V_{in}}\right| = \frac{A_o}{\sqrt{1 + \left(\frac{\omega_l}{\omega}\right)^{2n}}}$

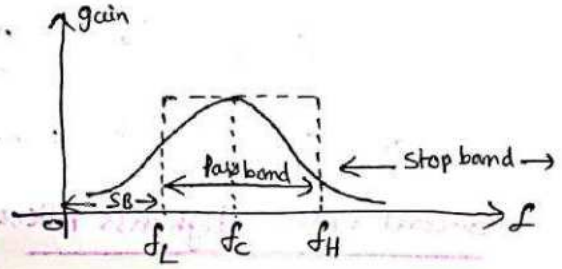
Band Pass Filter

A band pass Filter has a pass band between two cutoff frequencies f_H and f_L such that $f_H > f_L$. Any input frequency outside this passband is attenuated

There are two types of BPF

(1) Wide band pass Filter ($Q < 10$)

(2) Narrow band pass Filter ($Q > 10$)



The bellowing relationship are important:

$$\boxed{Q = \frac{f_0}{Bw} = \frac{f_0}{f_H - f_L}} \quad \text{and} \quad \boxed{f_c = \sqrt{f_H f_L}}$$

Wide Band Pass Filter

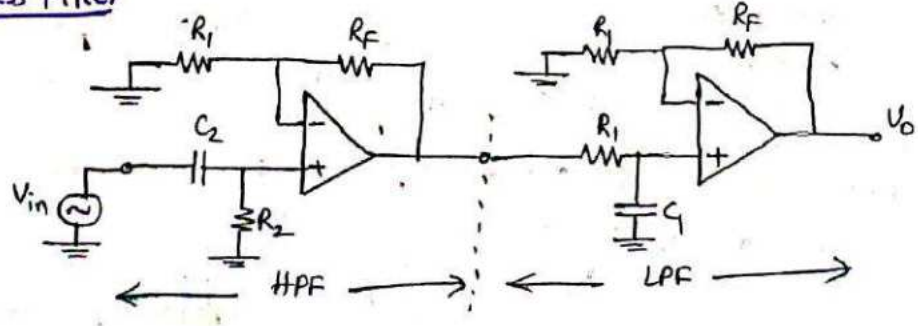


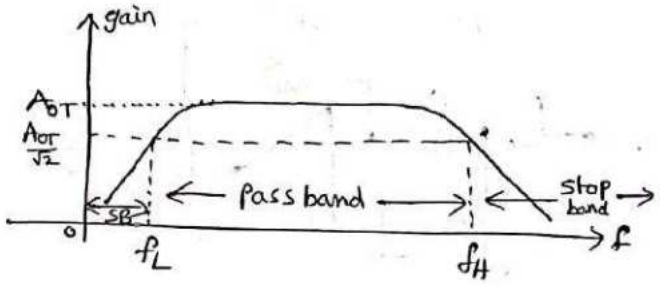
Fig:- Wide BPF.

A wide band pass Filter Can be formed by cascading a HPF and LPF. If the HPF and LPF are of the 1st order, then the BPF will have a roll-off rate of −20 dB/decade.

→ For LPF

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_{o1}\cdot f/f_L}{\sqrt{1+(f/f_L)^2}}$$

For HPF. $$\left|\frac{V_o}{V_{in}}\right| = \frac{A_{o2}}{\sqrt{1+(f/f_H)^2}}$$



Magnitude of gain of the wide band pass Filter is the product of individual gains of HPF and LPF.

$$\therefore \left|\frac{V_o}{V_{in}}\right| = \frac{A_{o1}\,(f/f_L)}{\sqrt{1+(f/f_L)^2}} \cdot \frac{A_{o2}}{\sqrt{1+(f/f_H)^2}} =$$

$$\boxed{\left|\frac{V_o}{V_{in}}\right| = \frac{A_{OT}\,(f/f_L)}{\sqrt{\left[1+(f/f_L)^2\right]\left[1+(f/f_H)^2\right]}}}$$

where, $A_{OT} = A_{o1}\cdot A_{o2}$ = Total Pass band gain.

$$f_L = \frac{1}{2\pi R_1 C_1}$$

$$f_H = \frac{1}{2\pi R_2 C_2}$$

Narrow Band pass Filter

The Narrow Band pass Filter using Multiple feedback is shown in figure. The op-amp is used in Inverting mode.

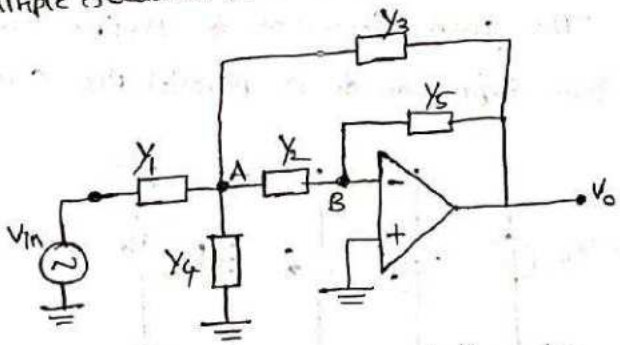


Fig:- Band pass Configuration.

Analysis ; $V_B = 0$

at node-A:

$$(V_A - V_{in})Y_1 + V_A Y_4 + (V_A - V_o)Y_3 + (V_A - V_B)Y_2 = 0$$

$$V_A(Y_1+Y_2+Y_3+Y_4) - V_o Y_3 = V_{in} Y_1 \rightarrow (1)$$

at node-B

$$(V_B - V_A)Y_2 + (V_B - V_o)Y_5 = 0$$

$$-V_A Y_2 - V_o Y_5 = 0 \Rightarrow V_A = -\frac{Y_5}{Y_2} V_o \rightarrow (2)$$

Substitute eq (2) in eq (1), we get

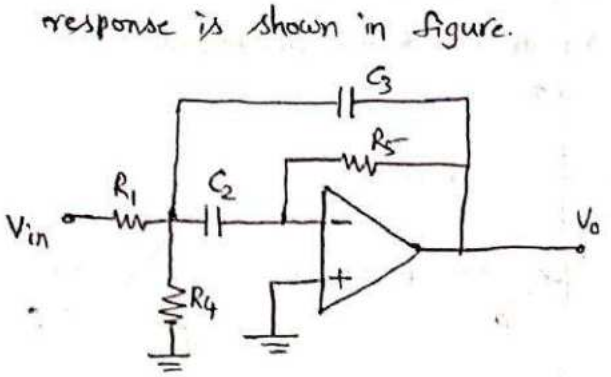
$$-\frac{Y_5}{Y_2} V_o (Y_1+Y_2+Y_3+Y_4) - V_o Y_3 = V_{in} Y_1$$

$$-V_o\left[\frac{Y_5}{Y_2}(Y_1+Y_2+Y_3+Y_4) + Y_3\right] = V_{in} Y_1$$

$$-V_o\left[\frac{Y_5(Y_1+Y_2+Y_3+Y_4) + Y_2 Y_3}{Y_2}\right] = V_{in} Y_1$$

$$\boxed{\frac{V_o}{V_{in}} = -\frac{Y_1 Y_2}{Y_5(Y_1+Y_2+Y_3+Y_4) + Y_2 Y_3}}$$

The Circuit Diagram of Multiple feedback Narrow Bandpass filter and its frequency response is shown in figure.



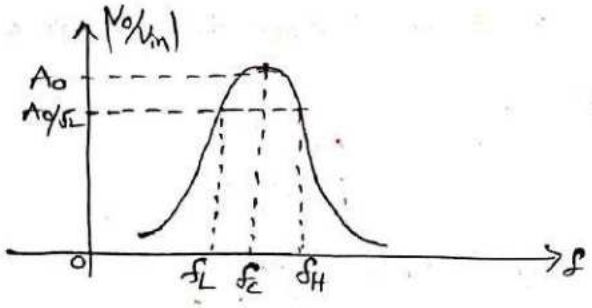


Fig:- Narrow Bandpass filter and its frequency response.

From the circuit by Comparison, we can write

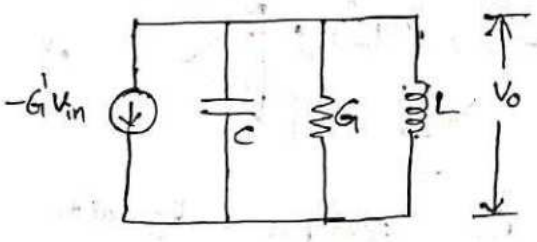
$$Y_1 = G_1,\ Y_2 = sC_2,\ Y_3 = sC_3,\ Y_4 = G_4 \text{ and } Y_5 = G_5.$$

$$\frac{V_o}{V_{in}} = -\frac{sC_2G_1}{s^2C_2C_3 + G_1G_5 + sC_2G_5 + sC_3G_5 + G_4G_5} = -\frac{sC_2G_1}{s^2C_2C_3 + s(C_2+C_3)G_5 + G_5(G_1+G_4)}$$

Divide both Numerator and Denominator by sC_2, we get

$$\boxed{\frac{V_o}{V_{in}} = \frac{-G_1}{sC_3 + \left(\frac{C_2+C_3}{C_2}\right)G_5 + \frac{G_5(G_1+G_4)}{sC_2}}} \rightarrow (1)$$

The gain Expression of Multiple feedback narrow bandpass filter is equivalent to the gain Expression of a Parallel RLC Circuit is driven by a current Source $-G'V_{in}$



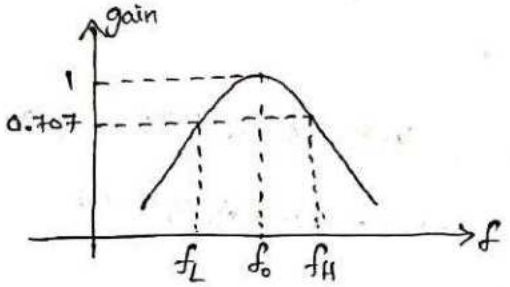


Fig:- A Parallel RLC Circuit and its Frequency response

$$\text{Gain, } \frac{V_o}{V_{in}} = \frac{-G'}{Y} = \frac{-G'}{sC + G + \frac{1}{sL}} \rightarrow (2)$$

By Comparing eq (1) & (2), we get

$$G' = G_1,\quad L = \frac{C_2}{G_5(G_1+G_4)},\quad G = G_5\frac{(C_2+C_3)}{C_2},\quad C = C_3$$

$$\Rightarrow \text{Resonant frequency, } \omega_0^2 = \frac{1}{LC} = \frac{1}{\left[\frac{C_2}{G_5(G_1+G_4)}\right]C_3} = \frac{G_5(G_1+G_4)}{C_2C_3}$$

$$\text{Gain at Resonance} = -\frac{G_1'}{G} = -\frac{G_1}{\left[\frac{G_5(C_2+C_3)}{C_2}\right]} = -\frac{G_1C_2}{G_5(C_2+C_3)}$$

$$\text{Quality Factor, } Q = \omega_0 RC = \frac{\omega_0 C}{G} = \frac{\omega_0 \cdot C_3}{G_5\left(\frac{C_2+C_3}{C_2}\right)} = \frac{\omega_0 C_2C_3}{G_5(C_2+C_3)}$$

$$\text{Band width} = f_H - f_L = \frac{f_0}{Q_0} = \frac{\omega_0}{2\pi Q}$$

$$= \frac{\omega_0}{2\pi\left[\frac{\omega_0 C_2 C_3}{(C_2+C_3)G_5}\right]} = \frac{G_5(C_2+C_3)}{2\pi C_2 C_3}$$

Center frequency, $f_0 = \sqrt{f_H f_L}$

Using Q, ω_0, $\frac{V_0}{V_{in}}$, gain at resonance,

$$\frac{V_0}{V_{in}} = \frac{-A_0\left(\frac{\omega_0}{Q}\right)s}{s^2+\left(\frac{\omega_0}{Q}\right)s+\omega_0^2} = \frac{-A_0\alpha\omega_0 s}{s^2+\alpha\omega_0 s+\omega_0^2}$$; where $\alpha = \frac{1}{Q}$ = Damping Factor

Note that for $\omega << \omega_0$ and $\omega >> \omega_0$, the gain is zero and for $\omega = \omega_0$, gain is A_0.

$\Rightarrow$ To Simplify Design Calculations, choose $C_1 = C_2 = C$.

(a) Gain at Resonance, $\frac{V_0}{V_{in}} = -\frac{G_1}{2G_5} \Rightarrow A_0 = \frac{G_1}{2G_5}$

(b) $\omega_0 = \frac{\sqrt{G_5(G_1+G_4)}}{C}$

(c) Band width $= \frac{G_5}{\pi C}$

(d) Quality factor, $Q = \frac{\omega_0 C}{2G_5}$.

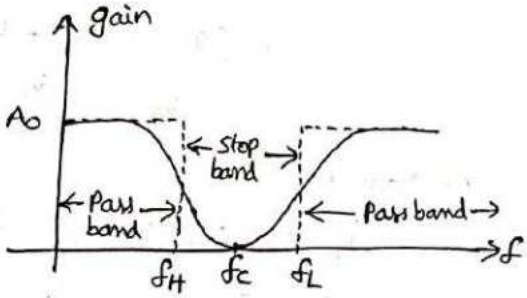
Band Reject Filter

Band reject filter stops or attenuates a specified band of frequencies. It is also called Band stop Filter (or) Band Elimination Filter.

Band Reject Filters are classified as

(1) wide band Reject Filter ($Q < 10$)

(2) Narrow Band Reject Filter ($Q > 10$)



Wide band Reject Filter

A wide band Reject Filter can be made by using a LPF, HPF and a Summer.

It is necessary that, (1) f_L of HPF should be much greater than f_H of LPF

(2) Pass band gain of LPF and HPF should be same.

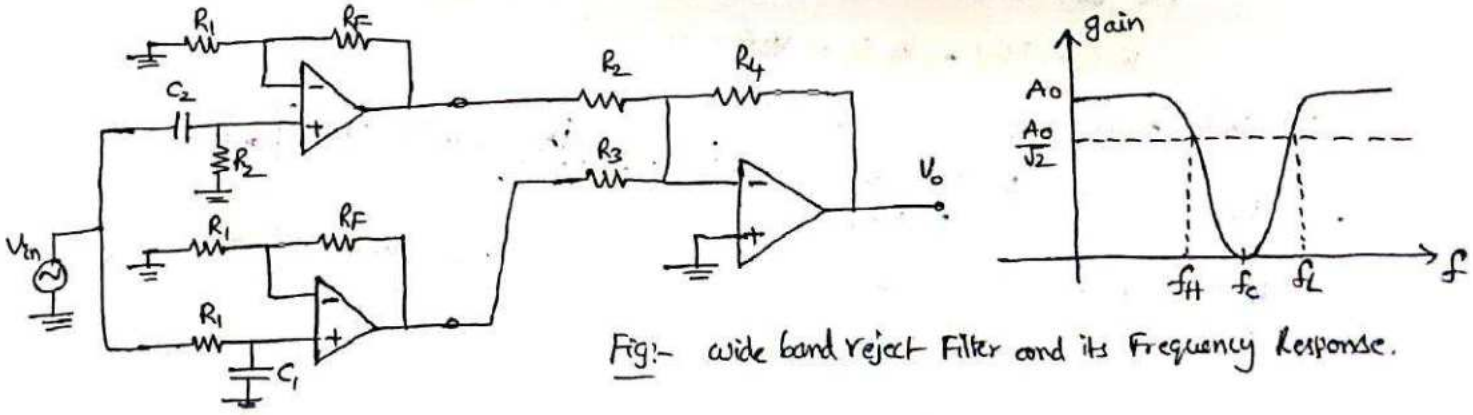


Fig:- wide band reject Filter and its Frequency Response.

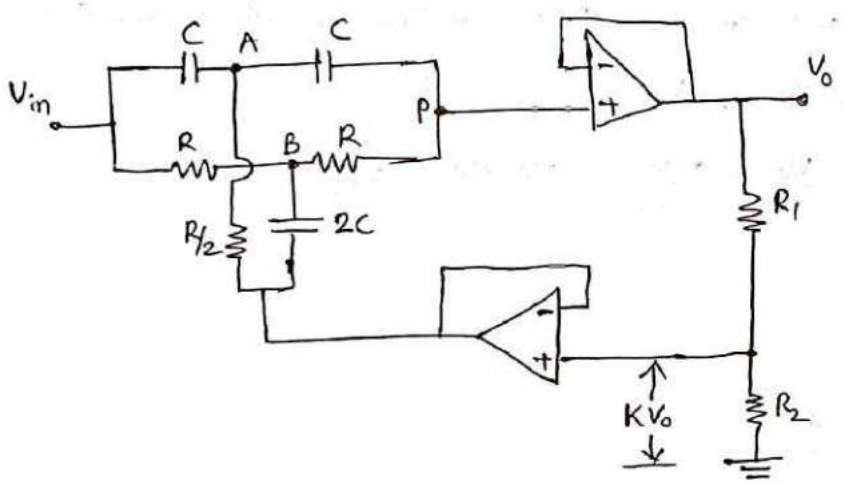
If the gain of the Summing amplifier is '1'. The overall transfer function of wide band reject filter can be written as

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_o}{\sqrt{1+\left(\frac{f}{f_H}\right)^2}} + \frac{A_o\left(f/f_L\right)}{\sqrt{1+\left(\frac{f}{f_L}\right)^2}} \quad ; \text{ where } f_L = \frac{1}{2\pi R_1 C_1} \text{ and } f_H = \frac{1}{2\pi R_2 C_2}.$$

Narrow Band Reject Filter

A Narrow band reject Filter is called as "Notch Filter". It is commonly used for the rejection of a single frequency such as 50 Hz power supply hum.

→ The most Commonly used notch Filter is the twin-T network.



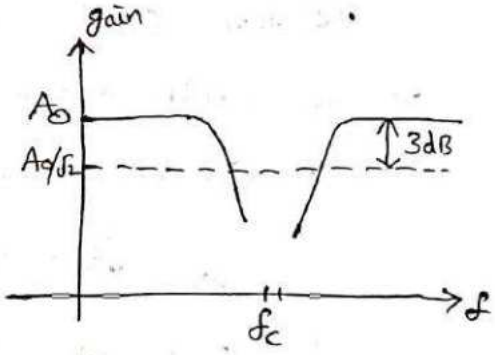


Fig:- Notch Filter and its Frequency response

where $K = \frac{R_2}{R_1+R_2}$

Analysis

At Node-A:

$$(V_A - V_{in})\,SC + (V_A - V_o)\,SC + (V_A - KV_o)\,2G = 0$$

$$V_A(2SC+2G) - V_{in}\,SC - V_o(SC+2KG) = 0$$

$$V_A = \frac{V_{in}\,SC + V_o(SC+2KG)}{2(SC+G)} \rightarrow (1)$$

At Node-B:

$$(V_B - V_{in})\,G + (V_B - V_o)\,G + (V_B - KV_o)\,2SC = 0$$

$$V_B(2G+2SC) - V_{in}\,G - V_o(G+2KSC) = 0$$

$$V_B = \frac{V_{in}\,G + V_o(G+2KSC)}{2(G+SC)} \rightarrow (2)$$

At Node-P:

$$(V_o - V_A)\,SC + (V_o - V_B)\,G = 0$$

$$V_o(SC+G) - V_A\,SC - V_B\,G = 0 \rightarrow (3)$$

Substitute eq① & ② in eq③, we get

$$V_o(SC+G) - \left[\frac{V_{in}\,SC + V_o(SC+2KG)}{2(SC+G)}\right]SC - \left[\frac{V_{in}\,G + V_o(G+2KSC)}{2(SC+G)}\right]G = 0$$

$$\frac{V_o\,2(SC+G)^2 - (V_{in}\,S^2C^2 + V_o\,S^2C^2 + V_o\,2KGSC) - (V_{in}G^2 + V_oG^2 + V_o\,2KGSC)}{2(SC+G)} = 0$$

$$V_o\left(2s^2c^2+2G^2+4scG-s^2c^2-2KGsc-G^2-2KGsc\right)-V_{in}\left(s^2c^2+G^2\right)=0$$

$$V_o\left[s^2c^2+G^2+4scG(1-K)\right]=V_{in}\left(s^2c^2+G^2\right)$$

$$\frac{V_o}{V_{in}}=\frac{s^2c^2+G^2}{s^2c^2+G^2+4scG(1-K)}$$

Divide both Numerator and denominator with c^2, we can write

$$\frac{V_o}{V_{in}}=\frac{s^2+(G/c)^2}{s^2+(G/c)^2+4s\frac{G}{c}(1-K)}$$

Let $\omega_o=\frac{1}{RC}=\frac{G}{c}$, $s=j\omega$, above equation can be written as

$$\frac{V_o}{V_{in}}=\frac{-\omega^2+\omega_o^2}{-\omega^2+\omega_o^2+j\,4(1-K)\omega\omega_o}=\frac{\omega^2-\omega_o^2}{\omega^2-\omega_o^2-j4(1-K)\omega\omega_o}\rightarrow(4)$$

At 3-dB points, $\left|\frac{V_o}{V_{in}}\right|=\frac{1}{\sqrt{2}}$

$$\therefore\quad \omega^2-\omega_o^2=\pm 4(1-K)\omega\omega_o$$

$$\omega^2\pm 4(1-K)\omega\omega_o-\omega_o^2=0$$

on solving quadratic equation, we get

$$f_L=f_o\left[\sqrt{1+4(1-K)^2}-2(1-K)\right]$$

$$f_H=f_o\left[\sqrt{1+4(1-K)^2}+2(1-K)\right]$$

The Bandwidth, $BW=f_H-f_L=4(1-K)f_o$

$$Q=\frac{f_o}{BW}=\frac{1}{4(1-K)}$$

As K approaches unity, Q factor becomes very large and BW approaches zero.

All Pass Filter

All Pass Filter passes all frequency components of the input signal without any attenuation and provides desired phase shift at different frequencies of the input signal.

When signals are transmitted over transmission lines, such as telephone lines, they undergo change in phase. These phase changes can be compensated by All Pass Filters. Thus all Pass Filters are also called Delay equalizers or phase correctors.

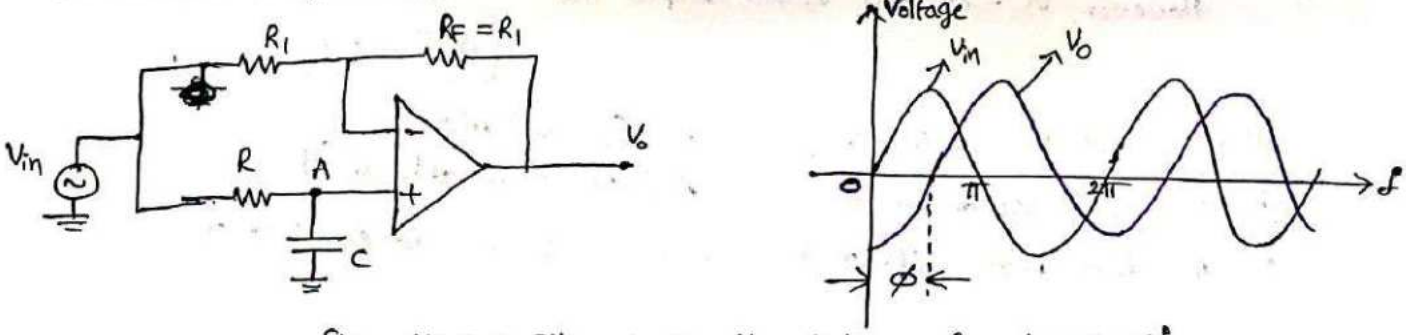


Fig:- All Pass Filter & its i/p and o/p waveform for $\phi=90^\circ$.

The output voltage, V_o is obtained by using the superposition theorem

$$V_o = -\frac{R_F}{R_1} V_{in} + \left(1+\frac{R_F}{R_1}\right) V_A \quad ; \quad V_A = \frac{\frac{1}{j\omega C} V_{in}}{R+\frac{1}{j\omega C}} = \frac{1}{1+j\omega RC} V_{in}$$

Since $R_F = R_1$, above equation can be written as

$$V_o = -V_{in} + 2\left(\frac{1}{1+j\omega RC}\right) V_{in} = V_{in}\left[-1 + \frac{2}{1+j\omega RC}\right]$$

$$V_o = V_{in}\left[\frac{-1-j\omega RC+2}{1+j\omega RC}\right] = V_{in}\left[\frac{1-j\omega RC}{1+j\omega RC}\right]$$

$$\left|\frac{V_o}{V_{in}}\right| = 1 \quad , \quad \phi = -2\tan^{-1}(\omega RC)$$

$\therefore |V_o| = |V_{in}|$, i.e, all i/p signal frequencies are passed by the Filter.

For fixed values of R and C, the phase angle varies between 0° to -180°.

Oscillators

An oscillator is a circuit that generates a repetitive waveform of fixed amplitude and frequency without any external input signal.

Basic principle of Oscillators

An oscillator is a feedback amplifier in which part of the o/p is feedback to the input via a feedback circuit. If the signal is fedback is of proper magnitude and phase, the circuit produces alternating currents or voltages.

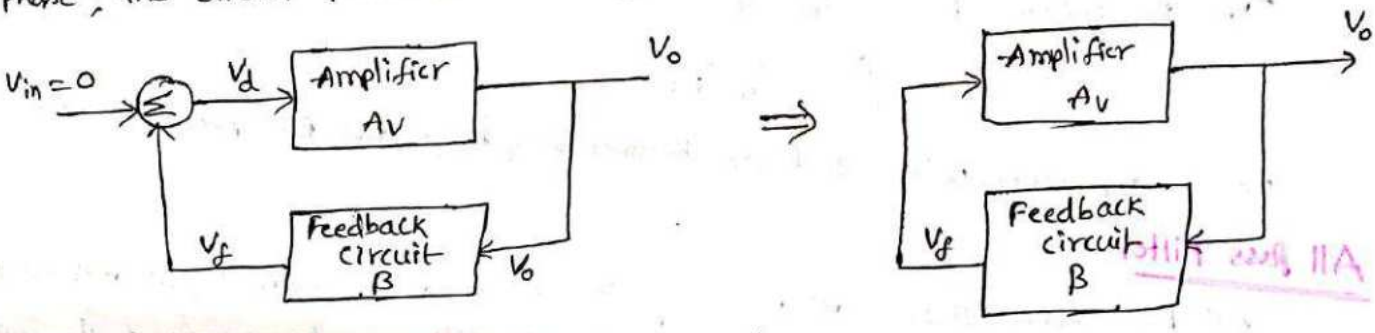


Fig: Oscillator block diagram

In the block diagram, $V_d = V_f + V_{in}$, $V_o = A_V V_d$, $V_f = \beta V_o$

From the above relationships, we get, $\boxed{\frac{V_o}{V_{in}} = \frac{A_V}{1-A_V\beta}}$

However, $V_{in}=0$ and $V_o \neq 0$ implies that, $A_V\beta = 1$ (or)

$\boxed{A_V\beta = 1 \angle 0^\circ \text{ or } 360^\circ}$

Above equation gives two requirements for oscillation.

1. The magnitude of the loop gain $A_V\beta$ must be atleast '1'.
2. The total phase shift of the loop gain $A_V\beta$ must be equal to 0° or 360°

Oscillator Types

Oscillators are classified as

1. Based on Type of Components used
   - RC oscillator
   - LC oscillator
   - Crystal oscillator
2. Based on Frequency of oscillation
   - Audio frequency (AF) oscillators
   - Radio frequency (RF) oscillators
3. Based on type of waveform generated
   - Sinusoidal
   - Square wave
   - Triangular wave
   - Sawtooth wave etc.

RC phase shift oscillator

The circuit of RC phase shift oscillator is shown in figure.

→ The op-amp is used in the inverting mode and therefore provides 180° phase shift. The additional phase of 180° is provided by the RC feedback network, to obtain a total phase shift of 360°.

The feedback network consists of three identical RC stages. Each stage provides a 60° phase shift. So that the total phase shift due to feedback network is 180°.

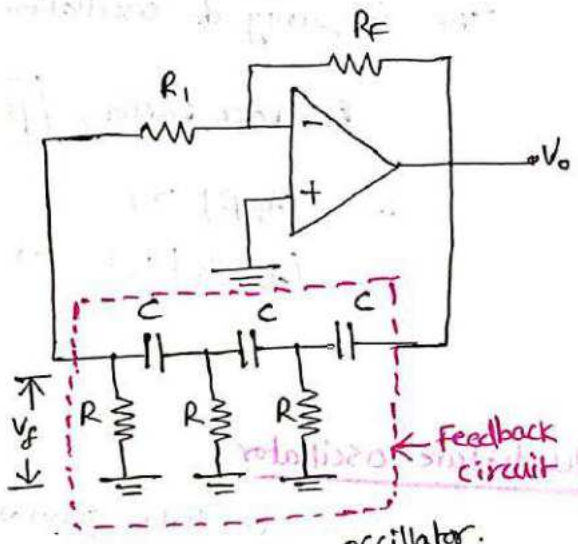


Fig:- RC phase shift oscillator.

At some specific frequency when the phase shift of the RC network is exactly 180° and the gain of the amplifier is sufficiently large, the circuit will oscillate at that frequency.

Frequency of oscillation, $\boxed{f_0 = \frac{1}{2\pi RC\sqrt{6}}}$

Feedback Factor, $\boxed{\beta = -\frac{1}{29}}$

$$|A_v\beta| \geq 1$$

$$|A_v(-1/29)| \geq 1 \Rightarrow |A_v| \geq 29.$$

$$|A_v| = \left|-\frac{R_F}{R_1}\right| \Rightarrow \frac{R_F}{R_1} = 29$$

$$\boxed{R_F = 29R_1}$$

Wien Bridge Oscillator

It is one of the most commonly used audio frequency oscillator.

→ Oscillator consists of series RC in one arm and parallel RC in another arm.

→ Feedback signal is connected to the non-inverting i/p terminal so that op-amp is working as Non-inverting amplifier.

Therefore the feedback network need not produce any phase shift.

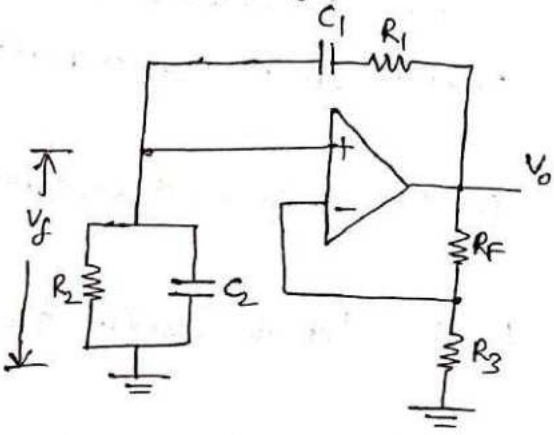


Fig:- Wien bridge oscillator

→ The condition of zero phase shift occurs only when the bridge is balanced.

The frequency of oscillation, $f_0 = \frac{1}{2\pi RC}$; if $R_1 = R_2 = R$, $C_1 = C_2 = C$.

Feedback Factor, $\beta = 1/3$

$\therefore |A_V \beta| \geq 1$

$|A_V \cdot 1/3| \geq 1 \Rightarrow A_V \geq 3$

$1 + \frac{R_F}{R_3} \geq 3$

$\frac{R_F}{R_3} \geq 2 \Rightarrow R_F = 2R_3$

Quadrature Oscillator

Quadrature oscillator generates two signals (Sine and Cosine) that are in quadrature i.e, out of phase by 90°. The output of A1 is labeled as a Sine and the output of A_2 is a Cosine. This oscillator require a dual op-amp and 3 RC combinations.

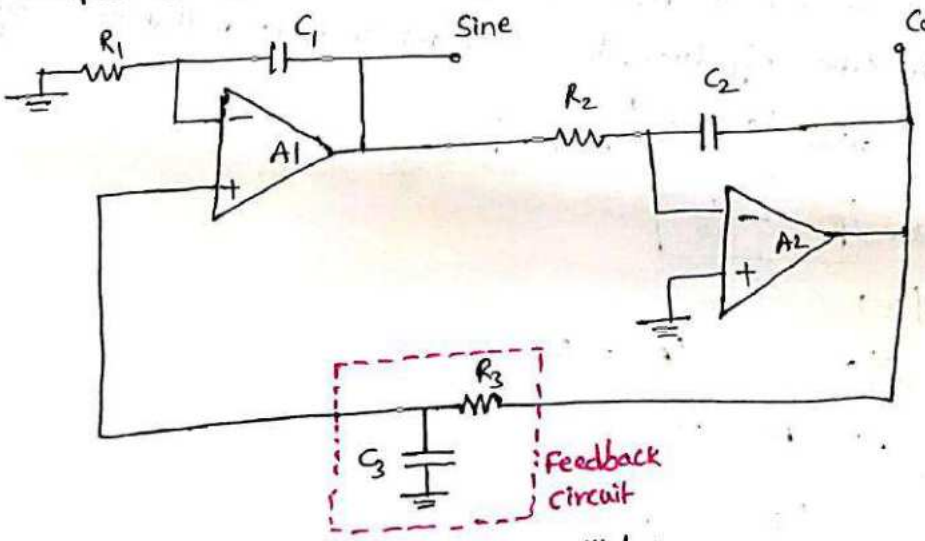


Fig:- Quadrature oscillator

The first op-amp A1 is operating in the non-inverting mode and appears as non-inverting integrator. The second op-amp A2 is working as a pure integrator.

→ when the wiper of R_4 is moved towards $+V_{cc}$, then fall time is longer than rise time.

→ Amplitude of Sawtooth wave is independent of the R_4 setting.

we know that $-V_r = -\frac{R_2}{R_3}(+V_{sat})$ and

$$+V_r = -\frac{R_2}{R_3}(-V_{sat})$$

$$\boxed{V_{opp} = (+V_r) - (-V_r) = \frac{2R_2}{R_3} V_{sat}}$$

→ The time taken by the o/p to swing from $-V_r$ to $+V_r$ is equal to T_1.

$$V_{opp} = -\frac{1}{(R_1+R_4)C_1}\int_0^{T_1}(-V_{sat})\,dt = \frac{V_{sat}}{(R_1+R_4)C_1}\cdot T_1$$

$$\therefore T_1 = \frac{(R_1+R_4)C_1 V_{opp}}{V_{sat}}$$

→ The time taken by the o/p to swing from $+V_r$ to $-V_r$ is equal to T_2.

$$V_{opp} = -\frac{1}{R_1C_1}\int_{T_1}^{T_2}(+V_{sat})\,dt = \frac{-V_{sat}}{R_1C_1}(T_2 - T_1)$$

$$T_2 - T_1 = -\frac{R_1C_1V_{opp}}{V_{sat}} \Rightarrow T_2 = T_1 - \frac{R_1C_1V_{opp}}{V_{sat}}$$

$$T_2 = -\frac{R_1C_1V_{opp}}{V_{sat}} + \frac{(R_1+R_4)C_1V_{opp}}{V_{sat}} = \frac{V_{opp}}{V_{sat}}R_4C_1$$

$\therefore$ Total Time, $T = T_1 + T_2 = \frac{(R_4+R_1)C_1V_{opp}}{V_{sat}} + \frac{V_{opp}R_4C_1}{V_{sat}}$

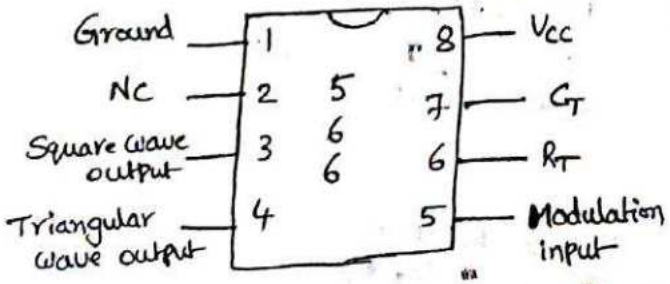
$$\boxed{T = (R_1C_1 + 2R_4C_1)\frac{V_{opp}}{V_{sat}}}$$

output frequency, $\boxed{f = \frac{1}{T} = \frac{V_{sat}}{V_{opp}}\left(\frac{1}{R_1C_1+2R_4C_1}\right)}$

Voltage Controlled oscillator (VCO)

A VCO is a circuit in which the frequency of oscillations depends on the amplitude of the voltage applied to its input. It is also known as voltage to frequency Converter.

The pin Configuration and block diagram of 566 Ic are shown in figure.



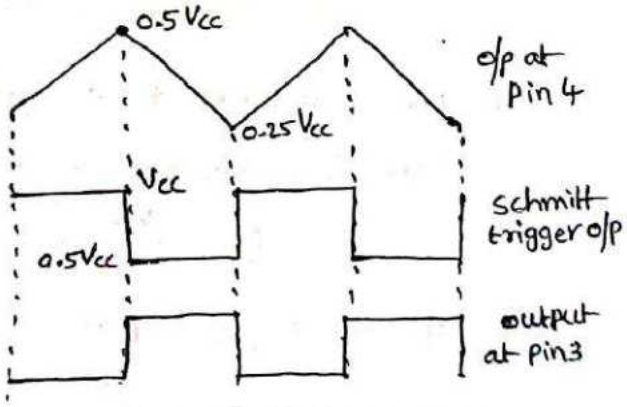


Fig:- pin Configuration & output waveforms.

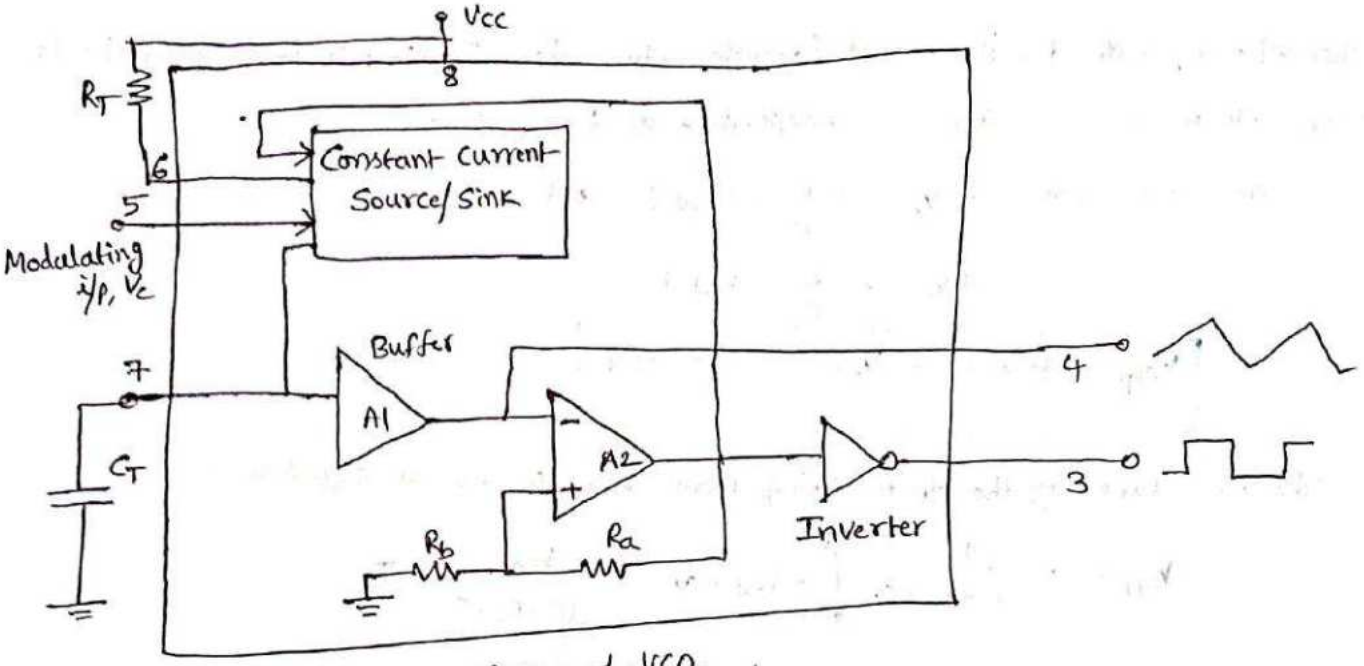


Fig:- Block Diagram of VCO.

A timing capacitor C_T is linearly charged or discharged by a constant current source/sink. The amount of current can be controlled by V_c applied at pin 5. or by changing R_T. If the voltage at pin 5 is increased, the voltage at pin 6 also increases, resulting in less voltage across R_T, thereby decreasing the charging current.

The voltage across C_T is applied to the (−) terminal of schmitt-trigger, A2. The o/p voltage of A2 is designed to V_{cc} and $0.5V_{cc}$.

If $R_a = R_b$, voltage at (+) terminal of A2 swings from $0.5V_{cc}$ to $0.25V_{cc}$. when the voltage across the capacitor exceeds $0.5V_{cc}$ during charging, the o/p of A2 goes low. Now the capacitor discharges to $0.25V_{cc}$. when it is at $0.25V_{cc}$, the o/p of A2 goes high. Since the source and sink currents are equal, capacitor charges and discharges for the same amount of time. This gives the triangular wave-form across C_T. and square wave can be obtained from the o/p of schmitt-trigger.

Frequency calculation

The voltage across the capacitor, C_T changes from $0.25V_{cc}$ to $0.5V_{cc}$

Thus $\Delta V = 0.25V_{cc}$. The capacitor charges with constant current source

$$I = C_T \frac{\Delta V}{\Delta t}$$

$$I = C_T\left(\frac{0.25V_{cc}}{\Delta t}\right) \Rightarrow \Delta t = \frac{0.25V_{cc}\,C_T}{I}$$

The total time period of triangular wave is, $T = 2(\Delta t)$.

The frequency of oscillation, $f_0 = \frac{1}{T} = \frac{1}{2(\Delta t)} = \frac{I}{0.5V_{cc}C_T}$; $I = \frac{V_{cc} - V_c}{R_T}$

$$f_0 = \frac{V_{cc} - V_c}{0.5V_{cc}R_TC_T} \rightarrow (1)$$

The o/p frequency of the VCO can be changed either by (1) R_T
(2) C_T
(3) V_c.

→ with no modulating i/p signal, if the voltage at pin 5 is biased at 7/8 V_{CC}

∴ VCO frequency is, $f_o = \frac{2(V_{CC} - 7/8\,V_{CC})}{0.5\,R_T C_T V_{CC}} = \frac{1}{4 R_T C_T} = \frac{0.25}{R_T C_T}$

Applications of VCO

(1) FM Modulation
(2) Triangular and Square wave generator
(3) FSK demodulator
(4) Frequency Multipliers

Problems

① Design a LPF at a cut-off frequency of 1KHz with a pass band gain of 2.

Sol:- $f_H = 1KHz = \frac{1}{2\pi RC}$

Let $C = 0.1\mu F$, then $R = \frac{1}{2\pi f C}$

$R = \frac{1}{2\pi \times 10^3 \times 0.1 \times 10^{-6}}$

$R = 1.59K\Omega$

Pass band gain, $A_o = 1 + \frac{R_F}{R_1} = 2$

$\frac{R_F}{R_1} = 2 - 1 = 1$

Let $R_1 = 10K\Omega$, then $R_F = 10K\Omega$

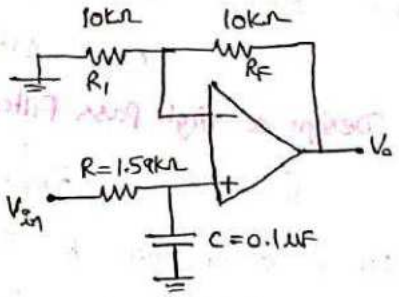


fig:- 1st order LPF

② Design a 2nd order Butterworth LPF having upper cut-off frequency 1 KHz.

Sol:- $f_H = 1KHz = \frac{1}{2\pi RC}$

Let $C = 0.1\mu F$, then $R = \frac{1}{2\pi \times 10^3 \times 0.1 \times 10^{-6}}$

$R = 1.59K\Omega$

For 2nd order LPF, polynomial is $(s^2 + 1.414s + 1)$

∴ $\alpha = 1.414 = 3 - A_o$

$A_o = 3 - \alpha = 3 - 1.414 = 1.586$

$A_o = 1 + \frac{R_F}{R_1} = 1.586$

$\frac{R_F}{R_1} = 1.586 - 1 = 0.586$

Let $R_1 = 10K\Omega$, then $R_F = 0.586 \times 10 \times 10^3 = 5.86K\Omega$

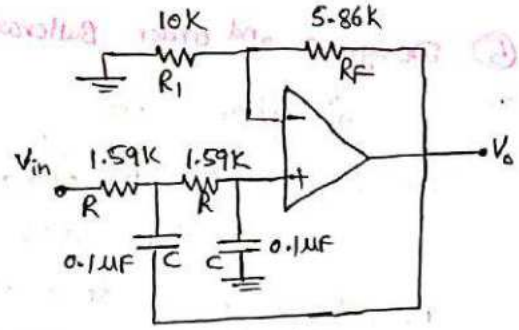


Fig:- 2nd order LPF

③ Design a 4th order Butterworth LPF having upper cut-off frequency 1KHz.

Sol:- $f_H = 1KHz = \frac{1}{2\pi RC}$

Let $C = 0.1\mu F$, then $R = \frac{1}{2\pi \times 10^3 \times 0.1 \times 10^{-6}}$

$R = 1.59K\Omega$

For 4th order, denominator polynomial is $(s^2 + 0.765s + 1)(s^2 + 1.848s + 1)$

∴ $\alpha_1 = 0.765 = 3 - A_{o1} \Rightarrow A_{o1} = 3 - 0.765 = 2.235$

$\alpha_2 = 1.848 = 3 - A_{o2} \Rightarrow A_{o2} = 3 - 1.848 = 1.152$

→ $A_{o1} = 1 + \frac{R_{F1}}{R_{11}} = 2.235 \Rightarrow \frac{R_{F1}}{R_{11}} = 2.235 - 1 = 1.235$

Let $R_{11} = 10\,k\Omega$, then $R_{F1} = 12.35\,k\Omega$

→ $A_{o2} = 1 + \frac{R_{F2}}{R_{12}} = 1.152 \Rightarrow \frac{R_{F2}}{R_{12}} = 1.152 - 1 = 0.152$

Let $R_{12} = 100\,k\Omega$, then $R_{F2} = 15.2\,k\Omega$

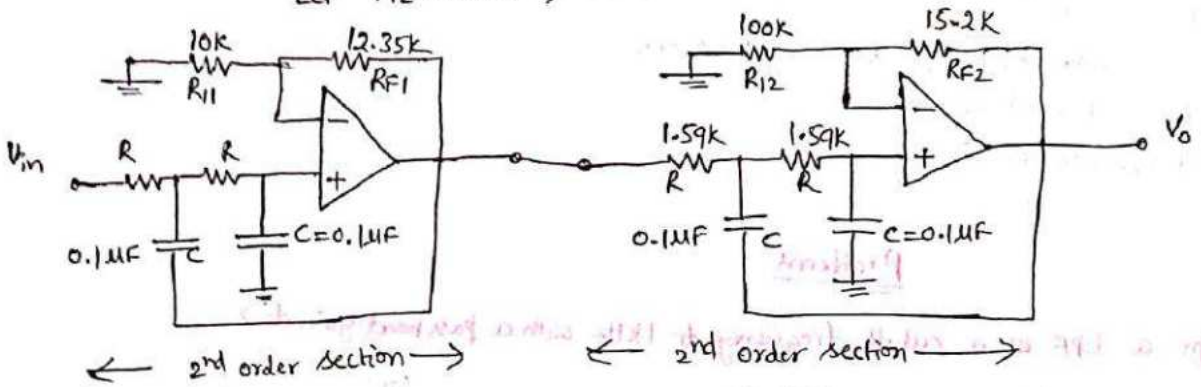


Fig:- 4th order Butterworth LPF

④ Design a high pass Filter at a cutoff frequency of 1KHz with a passband gain of 2.

Sol:- $f_L = 1\,KHz = \frac{1}{2\pi RC}$

Let $C = 0.1\mu F$, then $R = \frac{1}{2\pi f_L C}$

$$R = \frac{1}{2\pi \times 10^3 \times 0.1 \times 10^{-6}} = 1.59k\Omega$$

passband gain, $A_o = 1 + \frac{R_F}{R_1} = 2$

$$\frac{R_F}{R_1} = 1$$

Let $R_1 = 10k\Omega$, then $R_F = 10k\Omega$

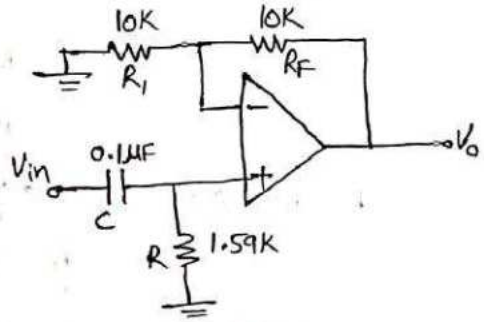


Fig:- 1st order HPF

⑤ Design a 2nd order Butterworth HPF having lower cutoff frequency 1KHz.

Sol:- $f_L = 1KHz = \frac{1}{2\pi RC}$

Let $C = 0.1\mu F$, then $R = \frac{1}{2\pi \times 10^3 \times 0.1 \times 10^{-6}}$

$$R = 1.59k\Omega$$

For 2nd order Filter, denominator polynomial $(s^2 + 1.414s + 1)$.

$\therefore \quad \alpha = 1.414 = 3 - A_o \Rightarrow A_o = 3 - \alpha = 3 - 1.414$

$$A_o = 1.586$$

$$A_o = 1 + \frac{R_F}{R_1} = 1.586$$

$$\frac{R_F}{R_1} = 1.586 - 1 = 0.586$$

Let $R_1 = 10k\Omega$, then $R_F = 5.86k\Omega$

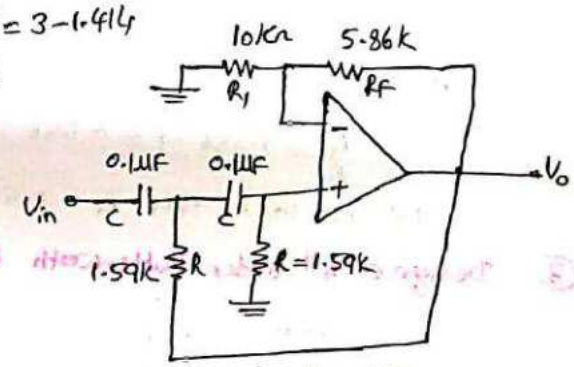
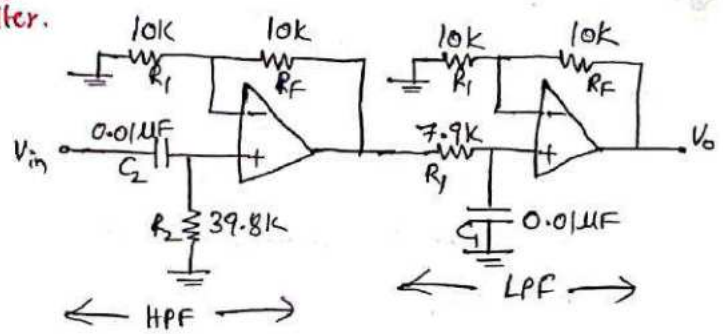


Fig:- 2nd order HPF

Note:- Design of higher order HPF is same as that of LPF design.

⑥ Design a wide-band pass filter having $f_L = 400$ Hz, $f_H = 2$ KHz and pass band gain of 4. Find the value of Q of the filter.



Sol:- Total Pass band gain = 4.

The LPF & HPF may be designed to give Pass band gain of 2.

$$A_o = 1 + \frac{R_F}{R_1} = 2$$

$$\frac{R_F}{R_1} = 1$$

Let $R_1 = 10K\Omega$, then $R_F = 10K\Omega$

→ for LPF, $f_H = 2\text{ KHz} = \frac{1}{2\pi R_1 C_1}$

Let $C_1 = 0.01\mu F$, then $R_1 = \frac{1}{2\pi f_H C_1} = \frac{1}{2\pi \times 2\times10^3 \times 0.01\times10^{-6}} = 7.9K\Omega$

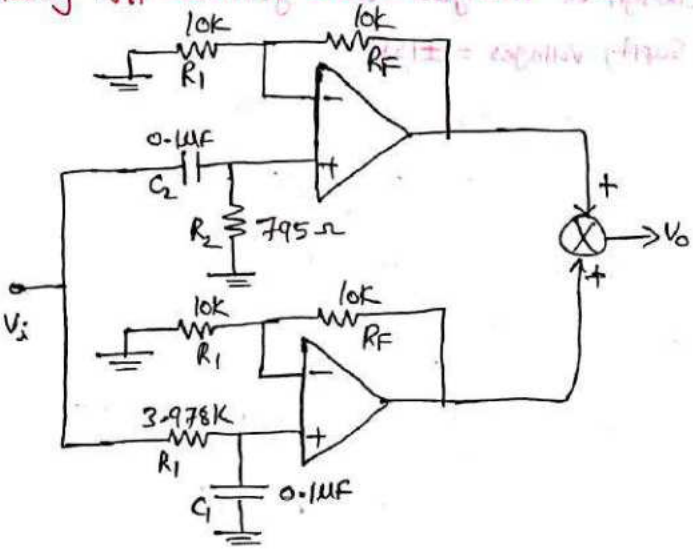
→ For HPF, $f_L = 400\text{ Hz} = \frac{1}{2\pi R_2 C_2}$

Let $C_2 = 0.01\mu F$, then $R_2 = \frac{1}{2\pi f_L C_2} = \frac{1}{2\pi \times 400 \times 0.01\times10^{-6}} = 39.8K\Omega$

$$f_o = \sqrt{f_H f_L} = \sqrt{2000 \times 400} = 894.4$$

$$Q = \frac{f_o}{BW} = \frac{894.4}{(2000-400)} = 0.56$$

⑦ Design a wide band reject filter having $f_H = 400$ Hz and $f_L = 2$KHz having Pass band gain of 2.



Sol:-

For HPF

$$f_L = 2\text{KHz} = \frac{1}{2\pi R_2 C_2}$$

Let $C_2 = 0.1\mu F$, then

$$R_2 = \frac{1}{2\pi \times 2000 \times 0.1\times10^{-6}} = 795\Omega$$

$$A_{o2} = 1 + \frac{R_F}{R_1} = 2$$

$$\frac{R_F}{R_1} = 1$$

Let $R_1 = 10K\Omega$, then $R_F = 10K\Omega$

For LPF

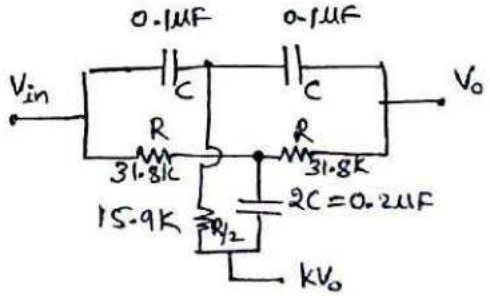
$$f_H = 400\text{ Hz} = \frac{1}{2\pi R_1 C_1}$$

Let $C_1 = 0.1\mu F$, then $R_1 = \frac{1}{2\pi \times 400 \times 0.1\times10^{-6}} = 3.978K\Omega$

$$A_{o1} = 1 + \frac{R_F}{R_1} = 2 \Rightarrow \frac{R_F}{R_1} = 1$$

Let $R_1 = 10K\Omega$, then $R_F = 10K\Omega$

⑧ Design a 50 Hz active Notch Filter.



Sol:-

$$f_o = 50\text{ Hz} = \frac{1}{2\pi RC}$$

Let $C = 0.1\mu F$, then $R = \frac{1}{2\pi \times 50 \times 0.1\times10^{-6}} = 31.8K\Omega$

(9) Design a Rc phase shift oscillator to oscillate at 100Hz

Sol:-

$$f_o = \frac{1}{2\pi RC\sqrt{6}} = 100$$

Let $C = 0.1\mu F$, then $R = \frac{1}{2\pi \times 100 \times \sqrt{6} \times 0.1\times10^{-6}}$

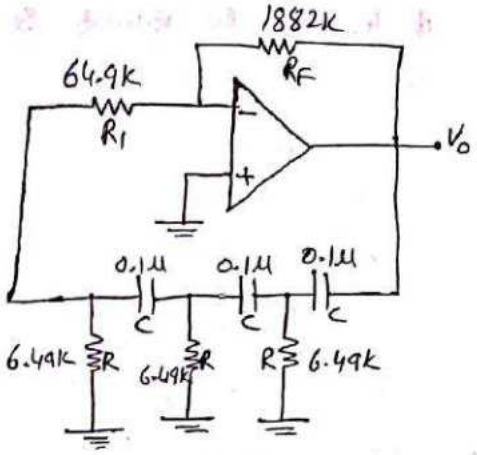
$$R = 6.49\,K\Omega$$

To prevent loading of the amplifier by Rc network,

$\boxed{R_1 \geq 10R}$

$R_1 = 10 \times 6.49K = 64.9K\Omega$

$\boxed{R_F = 29R_1} = 29 \times 64.9K = 1882\,K\Omega$



(10) Design a wien bridge oscillator with oscillation frequency of $f_o = 965$ Hz

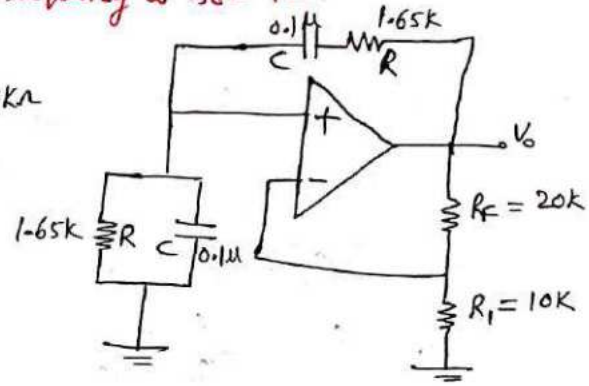
Sol:-

$$f_o = \frac{1}{2\pi RC} = 965\ Hz.$$

Let $C = 0.1\mu F$, then $R = \frac{1}{2\pi \times 965 \times 0.1\times10^{-6}} = 1.65K\Omega$

$\boxed{R_F = 2R_1}$

Let $R_1 = 10K\Omega$, then $R_F = 20K\Omega$



(11) Design a triangular wave generator with $f_o = 2KHz$ and $V_{opp} = 7V$. The op-amp power supply voltages $= \pm 15V$.

Sol:-

we know, $V_{opp} = \frac{2R_2}{R_3} V_{sat}$

$$7 = 2\frac{R_2}{R_3}(14) \Rightarrow R_2 = \frac{R_3}{4}$$

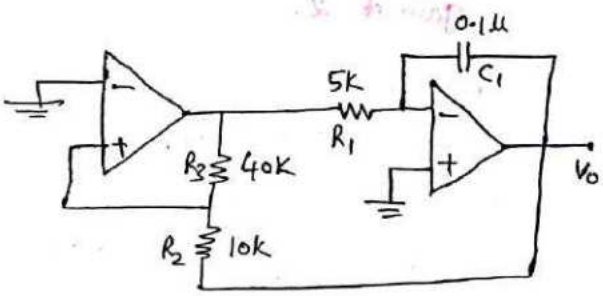
Let $R_2 = 10K\Omega$, then $R_3 = 40K\Omega$.

we have, $f_o = \frac{R_3}{4R_1C_1R_2}$

$$2000 = \frac{40\times10^3}{4R_1C_1 \times 10\times10^3} \Rightarrow R_1C_1 = 0.5\times10^{-3}$$

Let $C_1 = 0.1\mu F$, then $R_1 = \frac{0.5\times10^{-3}}{0.1\times10^{-6}} = 5K\Omega$

Note:- for op-amp with supply voltages $\pm V_{cc}$, $\pm V_{sat} = \pm(V_{cc} - 1)$



UNIT-II

Introduction to 555 Timer

→ The 555 timer is a highly stable device for generating accurate time delays or oscillations.

→ A single 555 timer can provide time delay ranging from micro seconds to hours.

→ It is available as an 8-pin DIP.

→ It operates on +5V to +18V supply voltages

→ It is compatible with both TTL and CMOS logic circuits

→ It can drive load upto 200mA.

Functional Diagram of 555 Timer

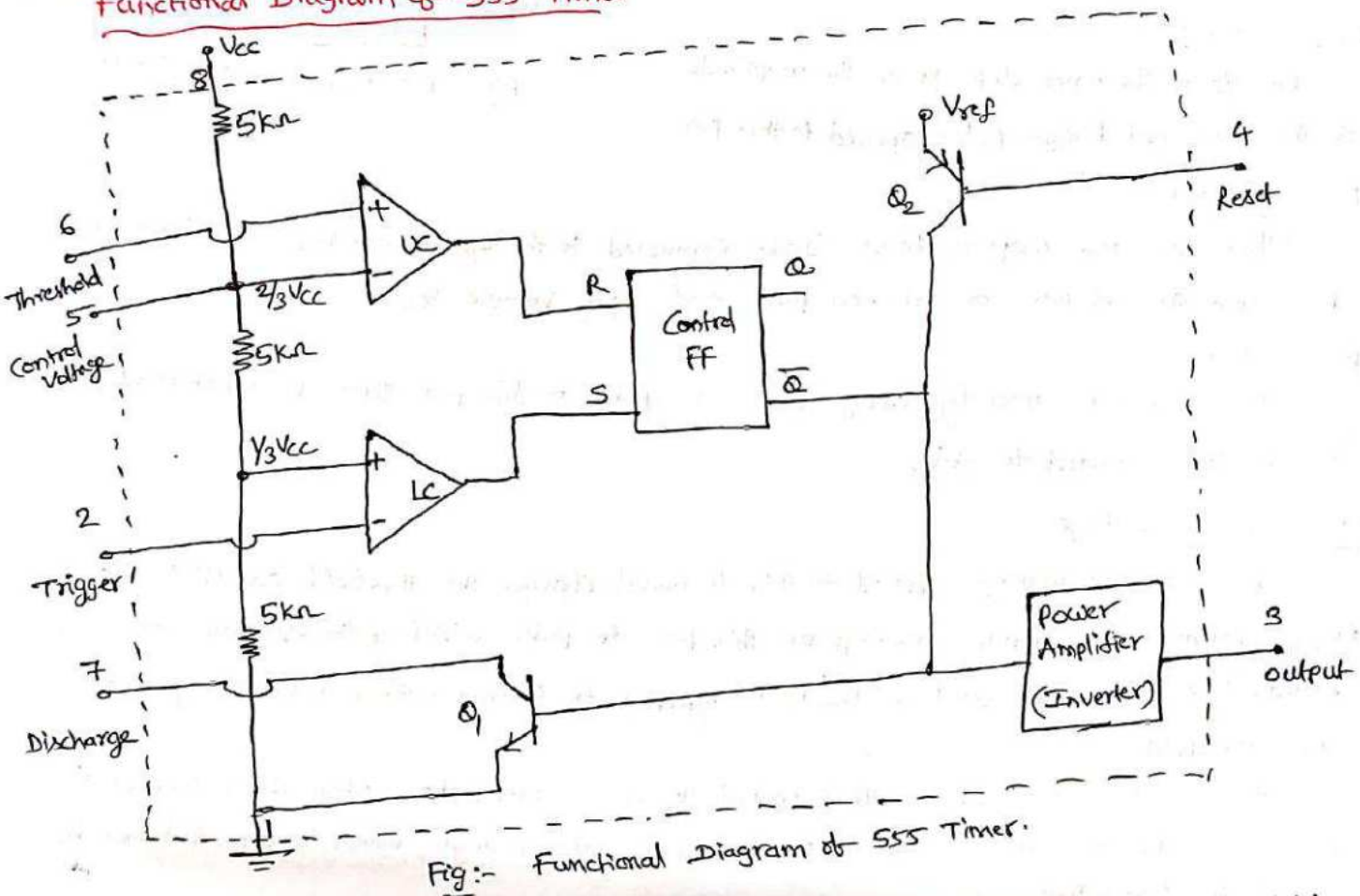


Fig:- Functional Diagram of 555 Timer.

⊛ In the figure, three 5 KΩ Resistors act as voltage divider, which provide bias voltage of $\frac{2}{3}V_{cc}$ to the upper comparator and $\frac{1}{3}V_{cc}$ to the lower comparator. These two voltages determine the time interval.

⊛ By applying modulation voltage to the control i/p terminal, we can vary the time.

⊛ In stand by state, $\overline{Q}$ of control flipflop is high. This makes the o/p low. A -ve trigger pulse is applied to pin2. As the trigger pulse passes through $\frac{1}{3}V_{cc}$, the o/p of the lower comparator is high and sets the flipflop ($Q=1$, $\overline{Q}=0$). when the voltage across the pin6 passes through $\frac{2}{3}V_{cc}$, the o/p of upper comparator

is high and Resets the Flipflop ($Q=0, \bar{Q}=1$).

- The Reset i/p provides a mechanism to reset the Flip Flop. The transistor Q_2 serves as a buffer to isolate the reset i/p from the Flipflop and transistor Q_1.
- when transistor Q_1 is ON, it provides the discharging path for the External Capacitor to ground. when it is off, pin 7 is open.

Pin diagram of 555 timer

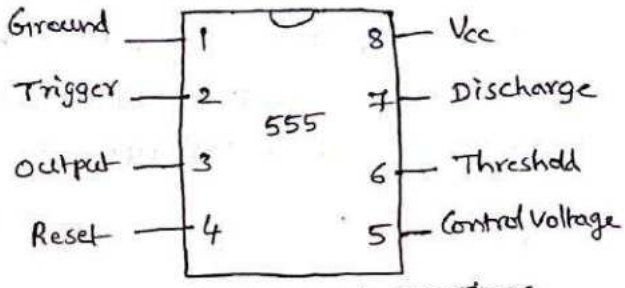


Fig:- Pin diagram of 555 Timer

Pin Functions :-

Pin1 – Ground:

All voltages are measured with respect to this terminal.

Pin2 – Trigger :

The o/p of the timer depends on the amplitude of the external trigger pulse applied to this pin.

Pin3 – output :

There are two ways a load Can be Connected to the o/p terminal, either between pin3 and ground. pin, or between pin3 and Supply voltage V_{cc}.

pin 4– Reset :

555 timer is reset by applying a -ve pulse to this pin. when it is not used it is usually Connected to $+V_{cc}$.

Pin5 – Control voltage :

An external voltage applied to this terminal Changes the threshold as well as the trigger voltage. By applying voltage on this pin, the pulse width of the o/p waveform Can be Varied. When it is not used, it should be bypassed to ground with a 0.01μf Capacitor.

Pin6 – Threshold :

This is the non-inverting i/p terminal of upper Comparator. when the voltage at this pin is greater than $\frac{2}{3}V_{cc}$, the o/p of upper Comparator is high, which in turn switches the o/p of the timer low.

Pin 7– Discharge :

This pin is internally Connected to the collector of transistor Q_1. when the o/p is high, Q_1 is off and act as an open circuit to the external Capacitor C Connected across it. when the o/p is low, Q_1 is act as short circuit for the external Capacitor 'C' to ground.

Pin 8 – +Vcc :

The Supply voltage of +5V to +18V is applied to this pin with respect to ground.

Monostable operation

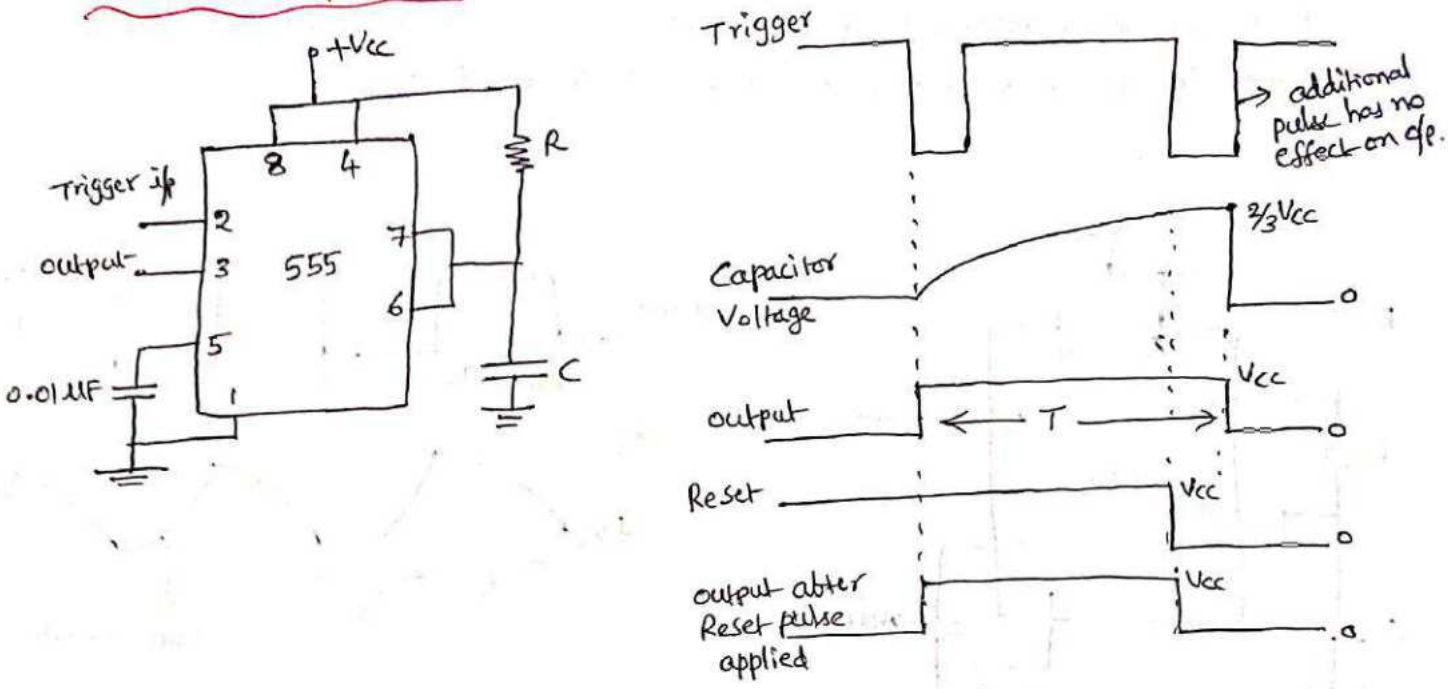


Fig:- Monostable Multivibrator and its waveforms

Operation

→ In standby state, Q_1 is ON clamping the external capacitor 'c' to ground. The o/p remain at ground potential i.e, low.

→ As the trigger pulse passes through $\frac{1}{3}V_{cc}$, the Flipflop is set ($\overline{Q}=0$). This makes Q_1 off and short circuit for the external capacitor is released. As $\overline{Q}$ is low, output goes high (V_{cc}).

The timing cycle now ~~repe~~ begins, voltage across the capacitor rises exponentially through R towards V_{cc} with a time constant RC. As the voltage across the capacitor is just greater than $\frac{2}{3}V_{cc}$, the upper comparator resets the Flip Flop. This makes $\overline{Q}=1$ and Q_1 is on, there by discharging 'c' to ground. The o/p returns to the standby state.

Calculation of Time Interval

The voltage across the capacitor can be written as, $V_c(t) = V_f + (V_i - V_f)\, e^{-t/RC}$

From figure, $V_i = 0$, $V_f = V_{cc}$, and at $t=T$, $V_c(t) = \frac{2}{3}V_{cc}$.

Therefore above equation can be written as

$$\frac{2}{3}V_{cc} = V_{cc} + (0 - V_{cc})\, e^{-T/RC}$$

$$\frac{2}{3}V_{cc} = V_{cc}\left[1 - e^{-T/RC}\right] \Rightarrow e^{-T/RC} = 1 - \frac{2}{3} = \frac{1}{3}$$

$$e^{T/RC} = 3 \Rightarrow T = RC\ln(3)$$

$$\boxed{T = 1.1RC}$$

Note:- ① Monostable Multivibrator is used to generate Variable pulse width.

② once multivibrator is triggered, the o/p remain in high state until time T. Any

additional trigger pulse during this time will not change the o/p state.

③ If a -Ve going reset pulse is applied to the Reset terminal, Q_1 becomes on and Capacitor 'C' is immediately discharged and o/p goes to Low.

Astable operation

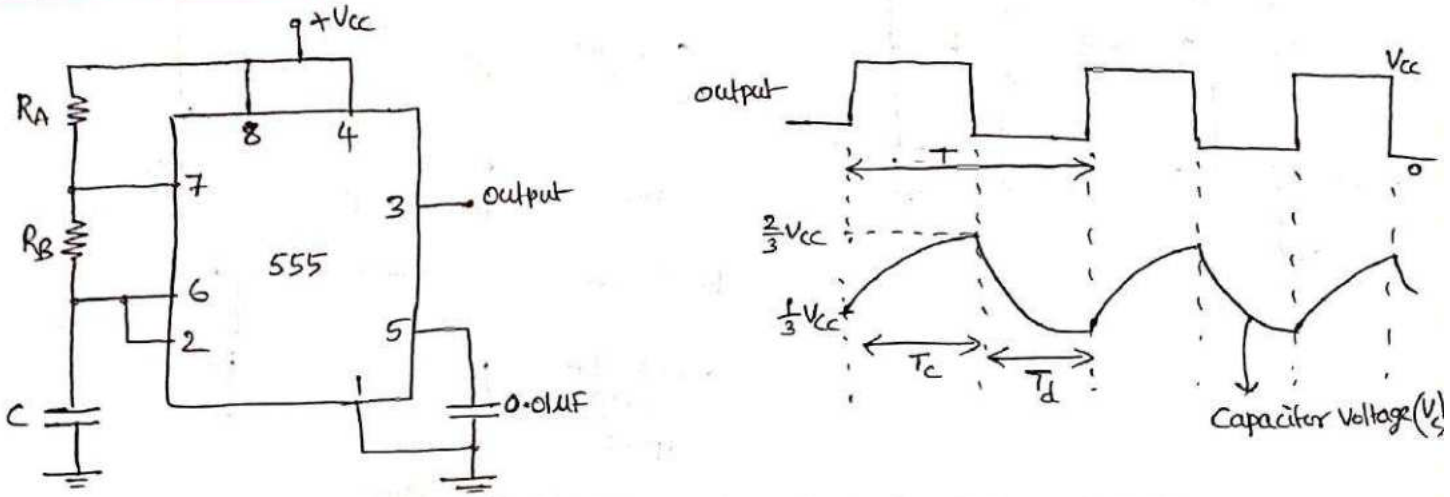


Fig:- Astable Multivibrator and its timing sequence.

operation :-

→ When the power supply V_{cc} is connected, the external Capacitor 'C' charges towards V_{cc} with a time constant $(R_A+R_B)C$. During this time o/p is high (S=1, R=0).

→ When the capacitor voltage just greater than $\frac{2}{3}V_{cc}$, the upper Comparator triggers the Flipflop so that $\bar{Q}=1$ and o/p is low. This makes Q_1 on and Capacitor 'C' starts discharging towards ground through R_B.

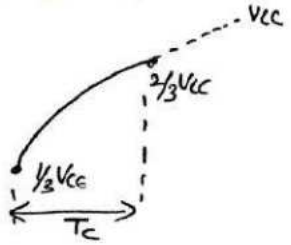
→ During the discharging of C, it reaches just less than $\frac{1}{3}V_{cc}$, the lower Comparator is triggered (S=1, R=0) which turns $\bar{Q}=0$ and o/p is High. Now Capacitor starts charge again.

Thus the Capacitor C is periodically charge and discharge between $\frac{1}{3}V_{cc}$ and $\frac{2}{3}V_{cc}$ and produces output shown in figure. It is also called free running oscillator.

Calculation of Free running Frequency

(a) Charging Time, T_c :

It is the length of time during which the o/p remains high. Time taken for the capacitor to charge from $\frac{1}{3}V_{cc}$ to $\frac{2}{3}V_{cc}$ may be calculated as



$$V_c(t) = V_f + (V_i - V_f)\, e^{-t/RC}$$

From figure, $V_i = \frac{1}{3}V_{cc}$, $V_f = V_{cc}$, at $t=T$, $V_c(t) = \frac{2}{3}V_{cc}$

$$\therefore \quad \frac{2}{3}V_{cc} = V_{cc} + (\tfrac{1}{3}V_{cc} - V_{cc})\, e^{\frac{-T_c}{(R_A+R_B)C}}$$

$$\frac{2}{3}V_{cc} = V_{cc}\left[1 - \frac{2}{3}\, e^{\frac{-T_c}{(R_A+R_B)C}}\right]$$

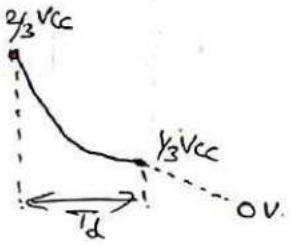
$$\frac{2}{3} e^{-T_c/(R_A+R_B)C} = 1 - \frac{2}{3} = \frac{1}{3}$$

$$\frac{2}{3} = \frac{1}{3} e^{\frac{T_c}{(R_A+R_B)C}} \Rightarrow T_c = (R_A+R_B)C \ln(2)$$

$$\boxed{T_c = 0.69 (R_A+R_B)C}$$

(b) Discharge time T_d:

It is the length of time during which o/p remain low. The time taken for the capacitor to discharge from $2/3 V_{cc}$ to $1/3 V_{cc}$ is calculated as



$$V_c(t) = V_f + (V_i - V_f) e^{-t/RC}$$

From figure, $V_i = 2/3 V_{cc}$, $V_f = 0$ V,

at $t = T_d$, $V_c(t) = 1/3 V_{cc}$

$$\therefore \frac{1}{3} V_{cc} = 0 + (2/3 V_{cc} - 0) e^{-T_d/R_BC}$$

$$\frac{1}{3} V_{cc} = \frac{2}{3} V_{cc} e^{\frac{-T_d}{R_BC}} \Rightarrow e^{\frac{T_d}{R_BC}} = 2$$

$$T_d = R_B C \ln(2)$$

$$\boxed{T_d = 0.69 R_B C}$$

$\therefore$ Total time period, $T = T_c + T_d$

$$= 0.69 (R_A+R_B)C + 0.69 R_B C$$

$$\boxed{T = 0.69 (R_A+2R_B) C}$$

$\therefore$ Free running frequency, $\boxed{f = 1/T = \frac{1.45}{(R_A+2R_B)C}}$

Duty cycle:

Duty cycle is defined as the ratio of "ON" time to the total time, T

$\therefore$ Duty cycle, $D = \frac{T_{ON}}{T} = \frac{T_c}{T}$

$$\therefore D = \frac{(R_A+R_B)C}{(R_A+2R_B)C} \Rightarrow \boxed{D = \frac{R_A+R_B}{R_A+2R_B}}$$

Astable Multivibrator with 50% Duty cycle

→ During the charging portion, diode D1 is forward biased and effectively short circuit R_B.

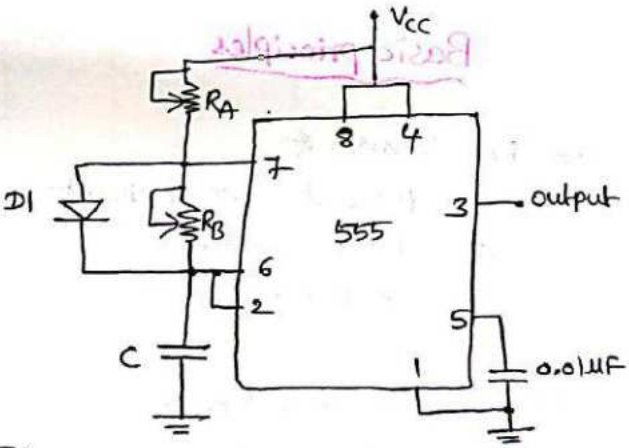
$\therefore T_c = 0.69 R_A C$.

⇒ During discharging portion, transistor Q_1 is on, discharges 'c' through R_B. and diode D1 is reverse biased.

$\therefore T_d = 0.69 R_B C$.

$\therefore$ Total time, $T = T_c + T_d = 0.69 (R_A+R_B)C$

Duty cycle, $D = \frac{T_c}{T} = \frac{0.69 R_A C}{0.69 (R_A+R_B)C} = \frac{R_A}{R_A+R_B}$.



→ At $R_A = R_B$, we get symmetrical square wave with 50% Duty cycle.

Schmitt Trigger

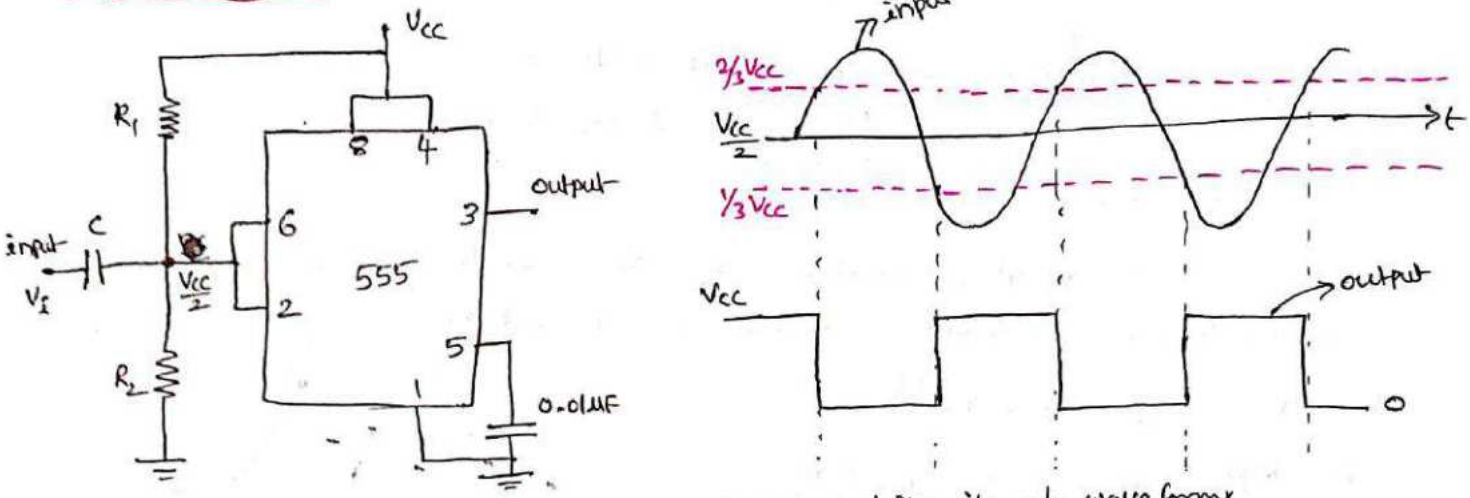


Fig:- Schmitt trigger and its i/p, o/p waveforms.

The 555 timer can be used as a schmitt-trigger as shown in figure.

⇒ Here two comparators are tied together and externally biased at $\frac{1}{2} V_{cc}$ through R_1 and R_2.

⇒ A Sine wave of sufficient amplitude $\left[> \frac{V_{cc}}{6} = \left(\frac{2}{3}V_{cc} - \frac{1}{3}V_{cc}\right)\right]$ exceed the reference levels and causes the internal Flipflop set and Reset, providing a square wave output as shown in figure.

Application of 555 Timer

1. Monostable and Astable Multivibrators
2. waveform generators
3. Traffic light Control
4. Tacho meters
5. Digital Logic probes

Phase Locked Loops

PLL was used for Radar synchronization and Communication applications. This technique of electronic frequency Control is used today in Satellite Communication systems, airborne navigational systems, FM Communication systems etc.

Basic principles

⇒ PLL Consists of
- (1) phase detector/Comparator
- (2) Lowpass Filter
- (3) Amplifier
- (4) VCO.

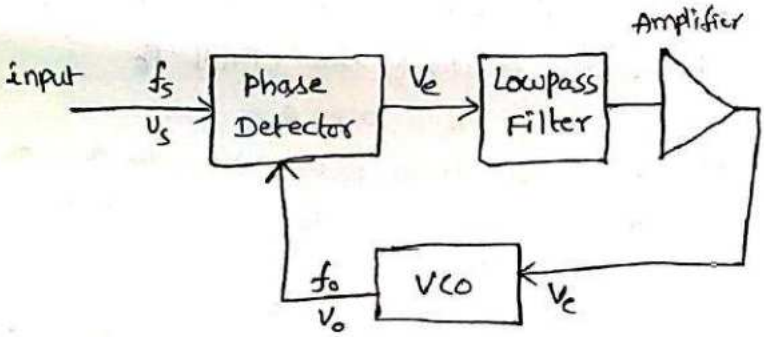


Fig:- Block schematic of PLL

⇒ The VCO is a free running Multivibrator operates at a frequency, f_o. This frequency is determined by Externally Connected Capacitor and Resistor.

operation :-

If an i/p signal V_s of frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the o/p of VCO. If the two signals differ in frequency or phase, an error voltage is generated. The phase detector is basically a multiplier and produces the sum (f_s+f_o) and difference (f_s-f_o) components at its output. The high frequency component is removed by the Lowpass Filter and the difference frequency component is ~~removed by the lowpass filter~~. amplified and then applied as control voltage to the VCO. The signal, V_c shifts the VCO frequency close to f_s. once this action starts, we say that the signal is in capture range.

The VCO continues to change the frequency till f_o is equal to f_s. except for a finite phase difference, ϕ. This phase difference generates a control voltage, V_c to shift VCO frequency from f_o to f_s and there by maintain lock. once locked, PLL tracks the frequency changes of the i/p signal.

Lock-in Range

The range of frequencies over which the PLL can maintain lock with the incoming signal is called the Lock-in range (or) track range

Capture-Range

The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range.

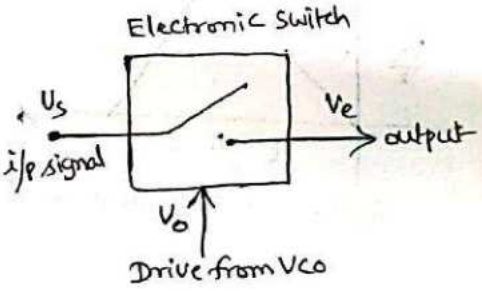
Pull-in time

The total time taken by the PLL to establish lock is called pull-in time.

Phase Detector/ Comparator

The phase detector is the most important part of the PLL system. There are two types of phase detectors. (1) Analog
(2) Digital

(a) Analog phase detector



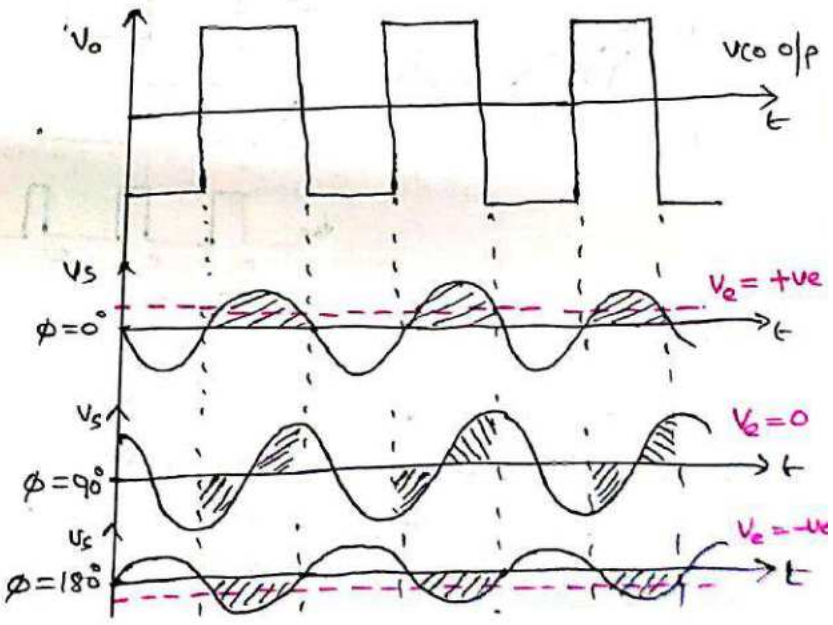


Fig:- phase detector and VCO, i/p waveforms for $\phi=0°, 90°, 180°$.

Figure represents the basic circuit and wave forms of analog phase detector. An electronic switch 'S' is opened and closed by signal coming from VCO. The i/p signal is therefore chopped at a repetition rate determined by VCO frequency.

⇒ When the i/p signal, V_s assumed to be in phase ($\phi = 0^\circ$) with V_o, error voltage is zero. The o/p waveforms for $\phi = 90^\circ$ and 180° are shown in figure. The o/p of phase detector is filtered through LPF, gives an error signal which is the average value of the o/p waveform.

It may be seen that error voltage is zero when the phase shift between the two inputs is 90°. So for perfect lock, VCO o/p should be 90° out of phase with the i/p signal.

Analysis

Phase detector is basically a multiplier, which multiplies the i/p signal by VCO signal.

Let $V_s = V_s \sin 2\pi f_s t$ and $V_o = V_o \sin(2\pi f_o t + \phi)$

$$\therefore V_e = K V_s V_o \sin 2\pi f_s t \sin(2\pi f_o t + \phi)$$

$$= K \frac{V_s V_o}{2} \left\{ \cos[2\pi(f_s - f_o)t - \phi] - \cos[2\pi(f_s + f_o)t + \phi] \right\}$$, where K = Comparator gain

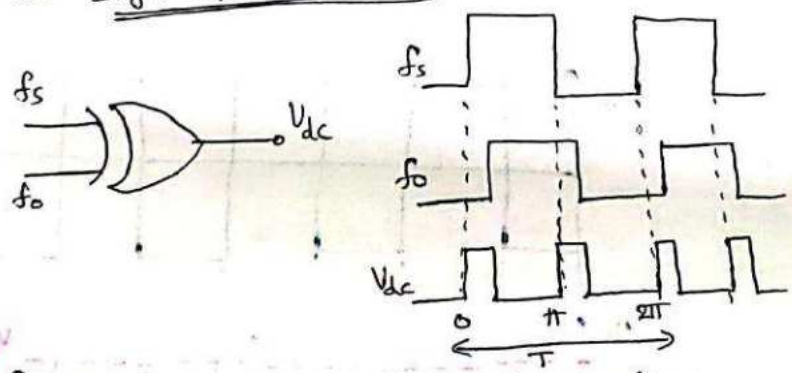
when at lock, $f_s = f_o$. Then

$$V_e = \frac{K V_s V_o}{2} \left[\underbrace{\cos\phi}_{DC} - \underbrace{\cos(4\pi f_o t + \phi)}_{\text{Double frequency term}} \right]$$

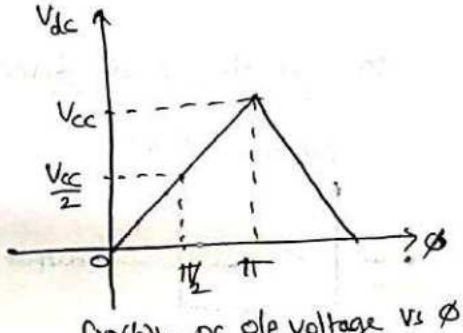
The double frequency term is eliminated by the Low pass filter and the DC signal is applied to the modulating i/p terminal of VCO.

⇒ It can be observed that $V_e = 0$ when $\phi = 90^\circ$.

(b) Digital phase Detector



fig(a):- Phase detector with i/p and o/p wave forms.



fig(b):- DC o/p voltage Vs φ.

The o/p of XOR gate is high only when one of its i/p signal is high. This type of detector is used when both i/p signals are square waves. From fig(b), we can observe that maximum dc o/p voltage occurs when the phase difference is π. The slope of the curve gives conversion ratio, K_ϕ of phase detector.

$$\therefore \boxed{K_\phi = \frac{V_{cc}}{\pi}} \text{ V/rad.}$$

Low pass Filter

The Filter used in PLL may be either passive or active.

The Low pass filter not only removes the high frequency components but also controls the dynamic characteristics of PLL. These characteristics include capture and lock range, bandwidth and transient response.

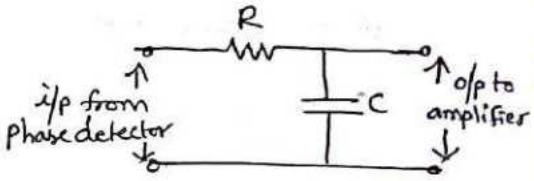
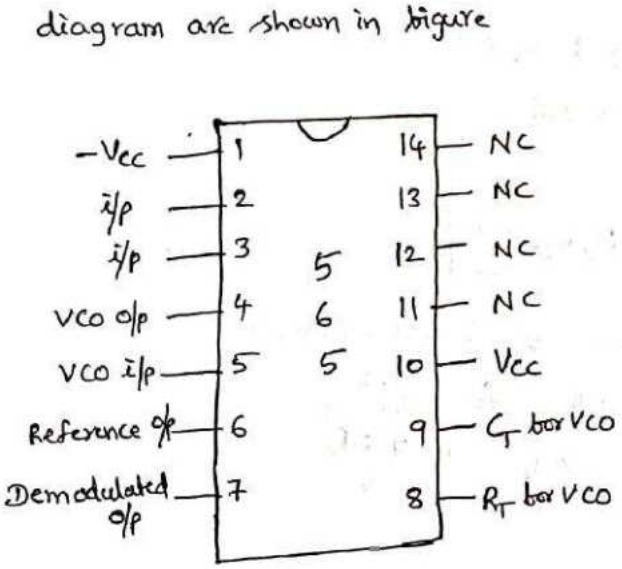


fig:- Passive LPF

if bandwidth is reduced, the transient time increases and capture range decreases. The charge on the capacitor gives a short time memory to the PLL. Thus even if the signal becomes less than noise for few cycles, the dc voltage on the capacitor continue to shift the VCO frequency till it picks up the signal again. This produces a high noise immunity and locking stability.

Monolithic phase Locked Loop (IC 565)

PLL IC 565 is available as a 14 pin DIP package. The pin configuration and block diagram are shown in figure



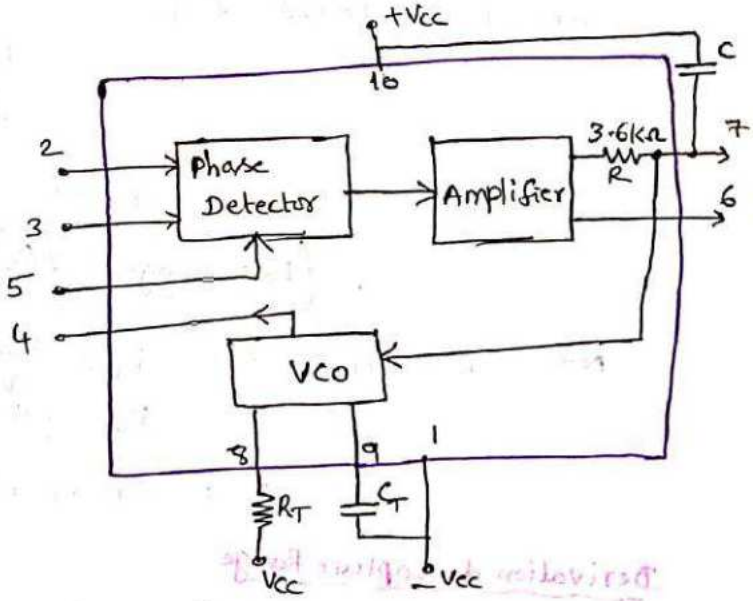


Fig:- IC 565 pin diagram and block diagram.

The VCO frequency is adjusted with R_T and C_T to be at the center of the i/p frequency range. Initially PLL is internally broken between the VCO o/p and phase comparator i/p. A short CKT between pin 4 and 5 compares f_o with f_s.

If an i/p signal is applied to the system, the phase comparator compares the phase and frequency of the i/p signal with the VCO frequency and generates an error voltage, V_e. The error voltage is then filtered, amplified and applied to the i/p of the VCO. The feedback nature of PLL causes the VCO to synchronize (or) lock to the incoming signal. once locked, VCO frequency is identical to the i/p signal, except for a finite phase difference.

Derivation of Lock-in Range:

If ϕ is the phase difference between the i/p signal and VCO frequency, then the o/p of the phase detector is $V_e = K_\phi (\phi - \pi/2)$

Control voltage, $V_c = A V_e = A K_\phi (\phi - \pi/2)$, where A = gain of the amplifier
K_ϕ = phase detector coefficient

This V_c shift the VCO frequency from its free running frequency f_0 to a frequency f.

$\therefore f = f_0 + K_V V_c$, where K_V = VCO coefficient.

$\Rightarrow$ The maximum o/p voltage available from the phase detector occurs for $\phi = \pi$ or 0

$\therefore V_{emax} = \pm K_\phi \pi/2$

$\therefore V_{cmax} = \pm \pi/2 K_\phi A.$

The maximum VCO frequency swing is given by $(f - f_0)_{max} = K_V V_{cmax}$

$$(f - f_0)_{max} = \pm K_V K_\phi A \pi/2$$

When PLL is locked, $f = f_s$.

$\therefore f_s = f_0 \pm K_V K_\phi A \pi/2$

$f_s = f_0 \pm \Delta f_L$

where, $\Delta f_L = K_V K_\phi A \frac{\pi}{2}$

$\therefore$ **Lock range** $= 2(\Delta f_L) = K_V K_\phi A \pi$

Note:- For PLL IC 565, $K_V = \frac{8 f_0}{V}$, where $V = (+V_{cc}) - (-V_{cc})$

$K_\phi \approx \frac{1.4}{\pi}$, $A = 1.4$, $f_0 = \frac{1.2}{4 R_T C_T}$

$\therefore$ Lock range becomes, $\Delta f_L = \pm \frac{7.8 f_0}{V}$

Derivation of Capture Range

The Lowpass Filter is a Simple RC network having transfer function.

$T(f) = \frac{1}{1 + j f/f_1}$, where $f_1 = \frac{1}{2\pi RC}$

when $(f/f_1)^2 >> 1$, $|T(f)| = \frac{f_1}{f}$

The frequency supplied by phase detector to LPF is $(f_s - f_0)$

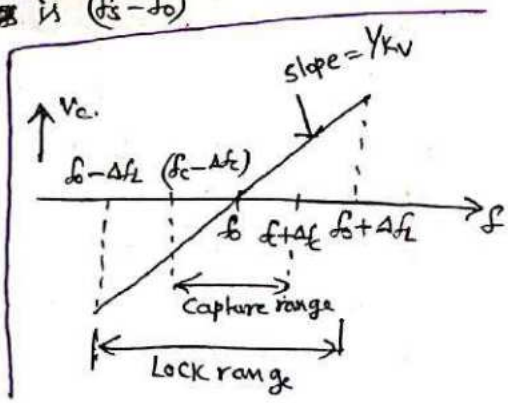
$V_{cmax} = A \cdot T(f) \cdot V_{emax}$

$= \pm K_\phi \frac{\pi}{2} \cdot A \cdot \frac{f_1}{(f_s - f_0)}$

The corresponding shift in VCO frequency is

$(f_s - f_0)_{max} = K_V V_{cmax} = \pm K_V K_\phi \frac{\pi}{2} A \frac{f_1}{(f_s - f_0)}$

$(f_s - f_0)^2 = \pm K_V K_\phi \frac{\pi}{2} A \cdot f_1$



$(\Delta f_c)^2 = K_v K_\phi \frac{\pi}{2} A f_1$, where $\Delta f_c = f_s - f_0$

$(\Delta f_c)^2 = \Delta f_L f_1$

$\boxed{\Delta f_c = \pm \sqrt{f_1 (\Delta f_L)}}$ or $\Delta f_c = \pm \sqrt{\frac{\Delta f_L}{2\pi RC}}$

Total capture range, $2\Delta f_c = 2\sqrt{f_1 (\Delta f_L)}$

PLL Applications

1. Frequency Multiplication or Division
2. Frequency Translation
3. AM Detection
4. FM demodulation
5. FSK Demodulator

Digital to Analog Converters (DAC)

Basic DAC Technique

→ i/p is a n-bit binary word, D and is combined with a reference voltage, V_R to give an analog o/p signal.

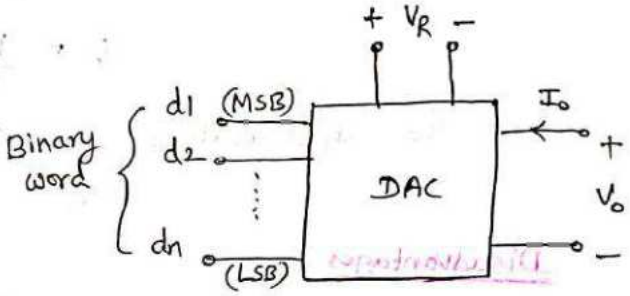


Fig:- Schematic of DAC

→ The o/p of DAC will be either voltage or current

→ For a voltage o/p DAC,

$$\boxed{V_o = K V_{FS} \left(d_1 2^{-1} + d_2 2^{-2} + \cdots\cdots + d_n 2^{-n}\right)} \rightarrow (1)$$

where, V_o = o/p voltage
V_{FS} = full scale o/p voltage
K = scaling factor usually adjusted to unity
d_1 = MSB with a weight of $\frac{V_{FS}}{2}$
d_n = LSB with a weight of $\frac{V_{FS}}{2^n}$.

There are various ways to implement equation (1),

1. Weighted Resistor DAC
2. R-2R Ladder DAC
3. Inverted R-2R Ladder DAC.

Weighted Resistor DAC

Circuit uses a Summing amplifier with a binary weighted Resistor network. It has 3 electronic switches d_1, d_2, d_3 Controlled by binary i/p word. These switches are SPDT type. If i/p is '1', it connects resistance to the reference voltage (V_R). If the i/p is '0', the switch connects the resistor to the ground.

Problems

① Design a Monostable Multivibrator using 555 timer to produce a pulse width of 8 ms.

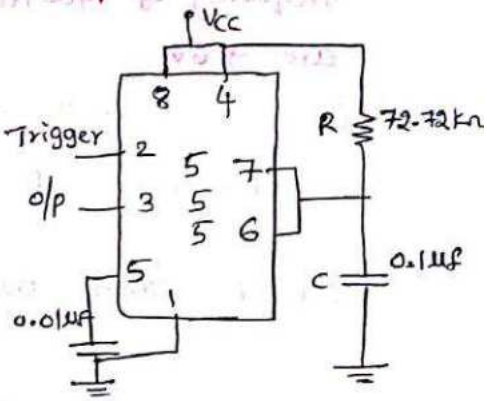
Sol:- Given that pulse width, $T = 8$ ms.

The pulse width Monostable Multivibrator is

$$\boxed{T = 1.1\,RC}$$

Let $C = 0.1\,\mu F$, then $8\times10^{-3} = 1.1(R)(0.1\times10^{-6})$

$$R = 72.72\,K\Omega$$



② A 555 timer is configured to run in Astable Mode with $R_A = 6.8\,K\Omega$, $R_B = 3.3\,K\Omega$ and $C = 0.1\,\mu F$. Determine the Free running frequency, Duty cycle, t_{high} and t_{low}.

Sol:- Given that, $R_A = 6.8\,k\Omega$, $R_B = 3.3\,k\Omega$, $C = 0.1\,\mu F$

$$t_{high} = t_c = 0.69(R_A + R_B)C = 0.69\,(6.8\times10^{3} + 3.3\times10^{3})(0.1\times10^{-6}) = 0.7\,ms$$

$$t_{low} = t_d = 0.69\,R_B C = 0.69\,(3.3\times10^{3})(0.1\times10^{-6}) = 0.23\,ms$$

Free running Frequency, $f = \dfrac{1.45}{(R_A+2R_B)C} = \dfrac{1.45}{(6.8\times10^{3}+2\times3.3\times10^{3})(0.1\times10^{-6})}$

$$f = 1.07\,KHz$$

Duty cycle, $D = \dfrac{R_A+R_B}{R_A+2R_B} = \left(\dfrac{6.8\times10^{3}+3.3\times10^{3}}{6.8\times10^{3}+2\times3.3\times10^{3}}\right)\times100\% = 75.3\%$

③ Design an Astable Multivibrator to generate the output signal with frequency of 2 KHz and Duty cycle of 60%.

Sol:- Given that $f = 2\,KHz$, $D = 60\% = 0.6$

$$D = \frac{R_A+R_B}{R_A+2R_B}$$

$$0.6 = \frac{R_A+R_B}{R_A+2R_B}$$

$$0.6R_A + 1.2R_B = R_A + R_B$$

$$0.2R_B = 0.4R_A$$

$$R_B = 2R_A \rightarrow (1)$$

We know $f = \dfrac{1.45}{(R_A+2R_B)C}$

Let $C = 0.1\,\mu F$, then

$$2\times10^{3} = \frac{1.45}{(R_A+2R_B)(0.1\times10^{-6})}$$

$$R_A+2R_B = \frac{1.45}{2\times10^{3}\times0.1\times10^{-6}} \rightarrow (2)$$

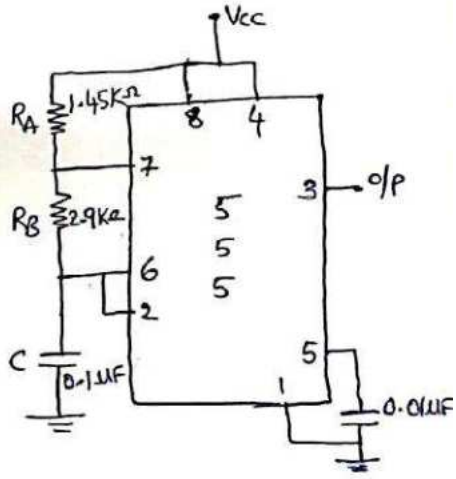
Substitute eq (1) in eq (2), we get

$$R_A + 4R_A = 7250$$

$$\boxed{R_A = 1.45\,K\Omega}$$

$$\therefore R_B = 2R_A = 2\times1.45K$$

$$\boxed{R_B = 2.9\,K\Omega}$$



④ Determine the values for R_1, C_1 and C_2 for LM 565 for a free running frequency of 400 KHz and a capture range of ± 10 KHz. The supply voltages are ± 6V.

Sol:- Given that, $f_0 = 400\,KHz$, $f_c = \pm 10KHz$, For 565 IC, $R_2 = 3.6k\Omega$

Free running frequency, $f_0 = \frac{1.2}{4R_1C_1}$

Let $R_1 = 10k\Omega$, then $C_1 = \frac{1.2}{4R_1 f_0} = \frac{1.2}{4\times10\times10^3\times400\times10^3} = 75\,Pf.$

Lock range, $f_L = \pm \frac{8f_0}{V} = \pm \frac{8\times400\times10^3}{6-(-6)} = \pm 266.66\,KHz$

Capture range, $f_c = \pm \sqrt{\frac{f_L}{2\pi R_2 C_2}}$

$$\pm(10\times10^3) = \pm \sqrt{\frac{266.66\times10^3}{2\pi\times3.6\times10^3\times C_2}} \Rightarrow C_2 = .0.11\mu f$$

⑤ Calculate the values of the LSB, MSB and Full scale output for an 8-bit DAC for the 0 to 10V range.

Sol:- $LSB = \frac{1}{2^8} = \frac{1}{256}$

For 10V range, $LSB = \frac{10}{256} = 39mV$

$MSB = \frac{1}{2}$.

For 10V range, $MSB = \frac{10}{2} = 5V$

Full Scale output = (Full scale Voltage − 1 LSB)

$= (10 - 39\times10^{-3}) = 9.961\,V$

⑥ What is the output voltage of the DAC for 0 to 10V range when the input binary number is (i) 10 (For a 2-bit DAC)
(ii) 0110 (For a 4-bit DAC)
(iii) 10111100 (For a 8-bit DAC)

Sol:- (i) $V_o = V_R(d_1\bar{2}^1 + d_2\bar{2}^2)$

$= 10(1\times\bar{2}^1 + 0\times\bar{2}^2) = 5V$

(ii) $V_o = V_R(d_1\bar{2}^1 + d_2\bar{2}^2 + d_3\bar{2}^3 + d_4\bar{2}^4)$

$= 10(0\times\bar{2}^1 + 1\times\bar{2}^2 + 1\times\bar{2}^3 + 0\times\bar{2}^4) = 3.75V$

(iii) $V_o = V_R(d_1\bar{2}^1 + d_2\bar{2}^2 + d_3\bar{2}^3 + d_4\bar{2}^4 + d_5\bar{2}^5 + d_6\bar{2}^6 + d_7\bar{2}^7 + d_8\bar{2}^8)$

$= 10(1\times\bar{2}^1 + 0\times\bar{2}^2 + 1\times\bar{2}^3 + 1\times\bar{2}^4 + 1\times\bar{2}^5 + 1\times\bar{2}^6 + 0\times\bar{2}^7 + 0\times\bar{2}^8) = 7.34V$

Voltage Regulator

The function of a voltage regulator is to provide a stable dc voltage for powering electronic circuits.

IC Voltage Regulators

IC voltage regulators are small in size, highly reliable, low cost and gives Excellent performance.

→ 78XX series are 3 terminal, +ve fixed voltage Regulators. There are 7 o/p voltage options available such as 5, 6, 8, 12, 15, 18 and 24 V. (XX) indicate the output voltage. Thus 7815 represents a 15V Regulator

→ 79XX Series gives −ve fixed voltage regulators.

723 General purpose Regulator

In IC 723 voltage regulator, o/p voltage can be adjusted over a wide range of both +ve and −ve voltage.

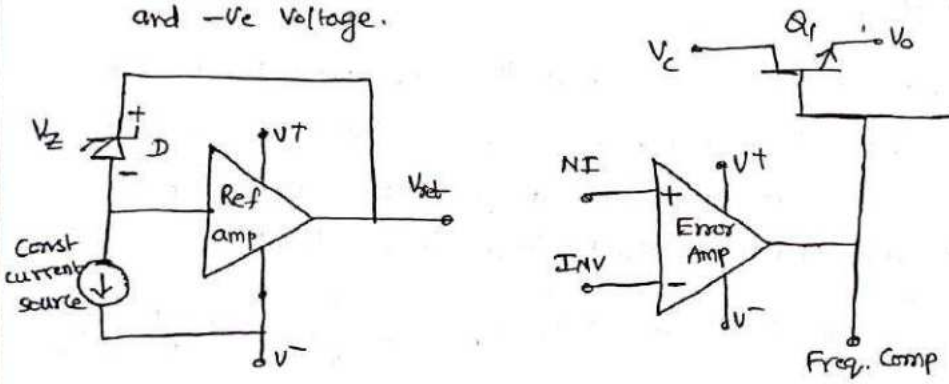
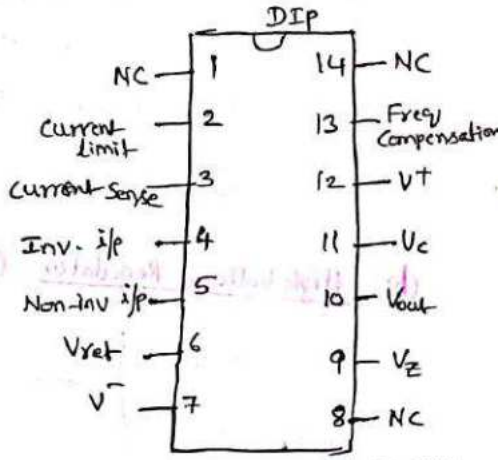


Fig:-(a) Functional block diagram of 723 Regulator



Fig(b):- PIN Diagram of Ic 723 Voltage Regulator.

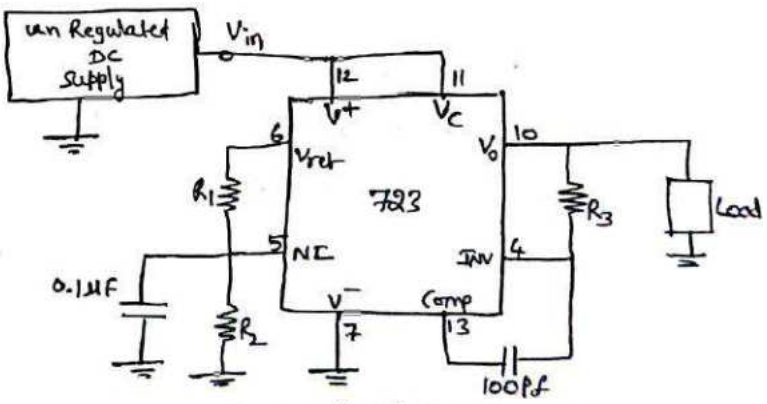
→ Figure (a) shows the functional block diagram of a 723 regulator IC.

The zener diode, a constant current source and reference amplifier produce a fixed voltage of about 7V at the terminal V_{ref}. The constant current source forces the zener to operate at a fixed point so that the zener outputs a fixed voltage.

→ The error amplifier compares a sample of the o/p voltage applied at the Inv i/p terminal to the reference voltage, V_{ref} applied at the NI i/p terminal. The error signal controls the conduction of Q_1 and hence it maintains constant o/p voltage. Ic 723 voltage regulator is available in 14 pin DIP as shown in fig(b).

(a) Low Voltage Regulator

A Simple +ve voltage (2 to 7V) regulator can be made using 723 as shown in fig.



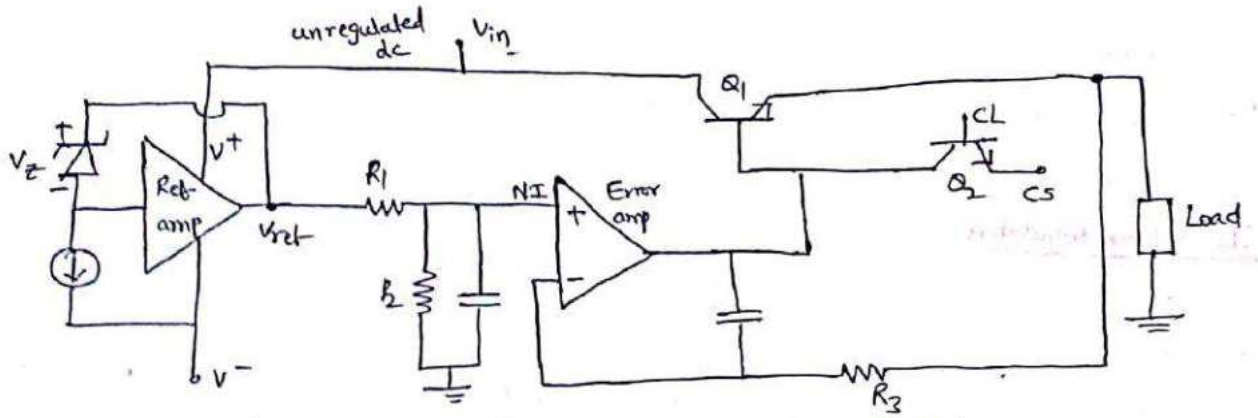


fig:- Functional diagram of a Low voltage Regulator.

Voltage at NI terminal of the Error amplifier due to R_1R_2 divider is, $V_{NI} = V_{ref}\frac{R_2}{R_1+R_2}$.

The difference between V_{NI} and the o/p voltage V_o which is directly fedback to the INV terminal is amplified by the Error amplifier. The o/p of the Error amplifier drives the transistor Q_1 so as to minimise the difference between the NI and INV inputs of Error amplifier. Since Q_1 act as Emitter follower; $\boxed{V_o = V_{ref}\frac{R_2}{R_1+R_2}}$

If the o/p voltage becomes low, the voltage at the INV terminal of error amplifier also goes down. This makes the o/p of the error amplifier to become more +ve, thereby driving transistor Q_1 more into Conduction. This increased current of transistor cause voltage across the load to increase. Similarly, any increase in load voltage get regulated.

The reference voltage is typically 7-15V. So the o/p voltage, $\boxed{V_o = 7.15\frac{R_2}{R_1+R_2}}$.

(b) High Voltage Regulator (>7V)

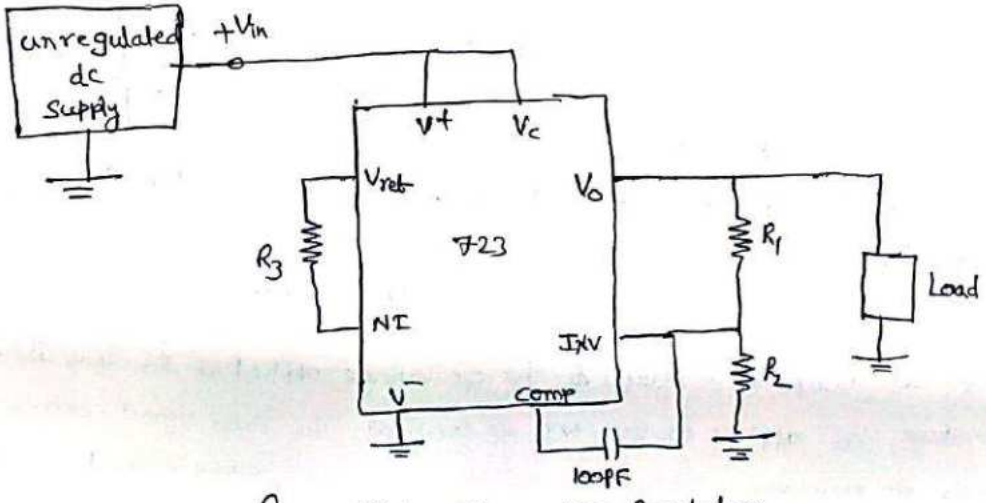


fig:- High voltage 723 Regulator

The above circuit is used to produce o/p voltage greater than 7V. The NI terminal is connected directly to V_{ref} through R_3. So the voltage at the NI terminal is V_{ref}. The error amplifier operates as a non-inverting amplifier with a voltage gain of $A_V = 1+\frac{R_1}{R_2}$.

So the output voltage for the circuit is $\boxed{V_o = 7.15\left(1+\frac{R_1}{R_2}\right)}$