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NANOSTRUCTURED PHOTOCATALYSTS

From Fundamental to Practical Applications

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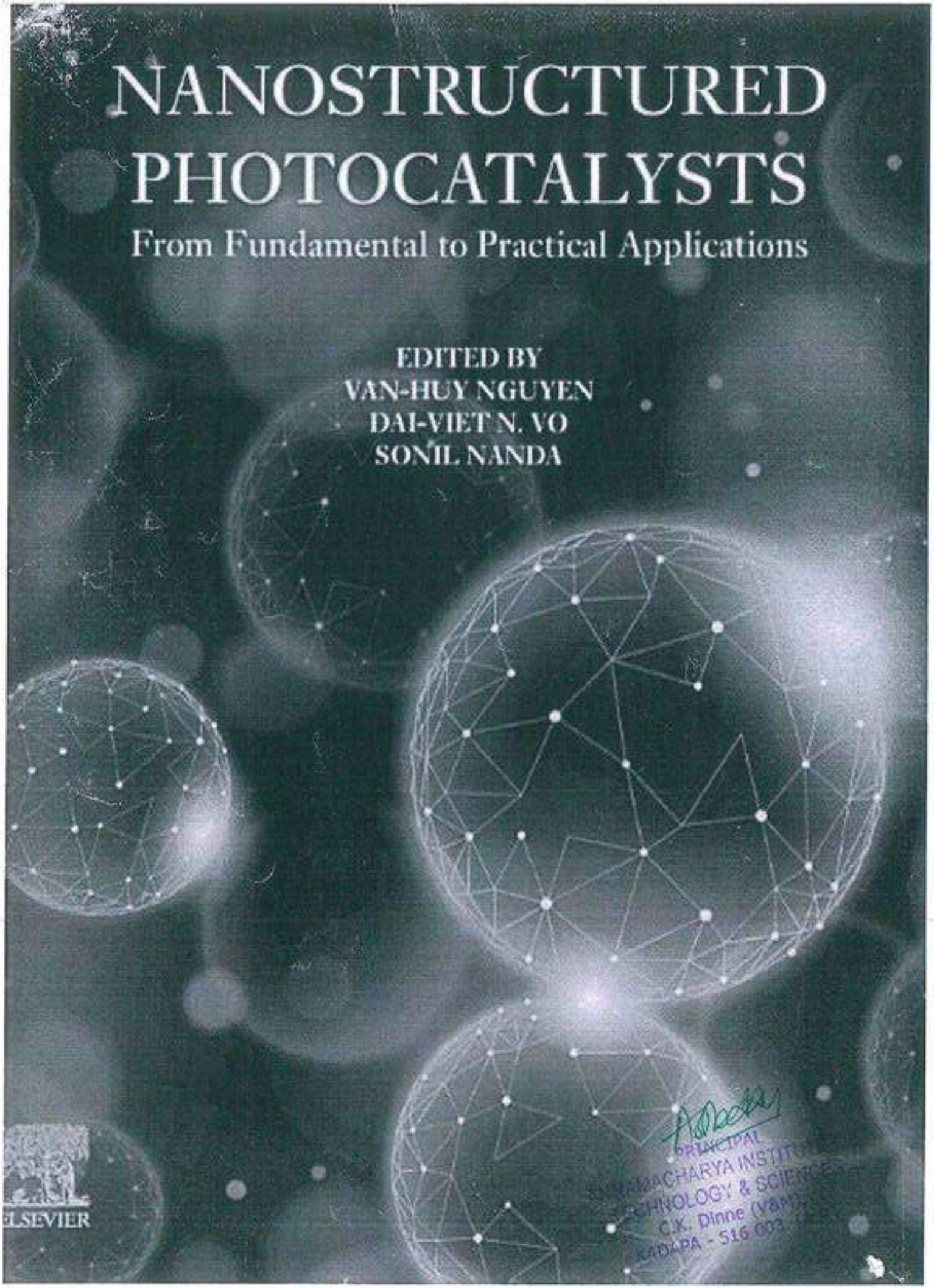

ELSEVIER

Nanostructured Photocatalysts
From Fundamental to Practical Applications

2021, Pages 489-517

Chapter 17 - Prospects and challenges of photocatalysis for degradation and mineralization of antiviral drugs

Lan-Anh Phan Thi [a, b], Sri Chandana Panchangam [c], Huu-Tuan Do [d], Van-Huy Nguyen [e]

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Abstract

Among the outbreak of influenza and other pandemics such as SARS-CoV-2 recently over the globe, antiviral drugs were significantly concerned with controlling the disease and these pandemics. They have been developed for seven decades around more than 90 drugs categorized licensed to treat nine human infectious diseases. Based on their functional group, antiviral compounds will mitigate infectivity and symptoms and reduce the illness period by arresting the viral replication cycle at different stages. Antiviral drugs have been developed complexly and met many biothreat challenges due to their high biosafety level requirement. In recent years, the spreading of novel virus strains that are a threat to human life, the development in researching a

CHAPTER

17

Prospects and challenges of photocatalysis for degradation and mineralization of antiviral drugs

Lan-Anh Phan Thi[a,b], *Sri Chandana Panchangam*[c], *Huu-Tuan Do*[d], *and Van-Huy Nguyen*[e]

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17.1 Introduction

Antiviral drugs are a specific class of medications used to treat a selective or broad spectrum of viral infections. Usually, viral infections resolve themselves if the virus that attacked humans is immune competent. However, incessantly, the world is witnessing the surge of viral infections ending up as either an epidemic or a pandemic. Among the outbreak of influenza and other pandemics such as SARS-CoV-2 recently over the globe, viral infections have been known as a significant reason for one group of death worldwide (Beck et al., 2020; Vahidnia et al., 2017). The development of antiviral drugs was significantly concerned with controlling the disease due to viral infections. In 1963, idoxuridine was recognized as the first antiviral compound by the US Food and Drug Administration (FDA) for the treatment of herpes simplex virus (HSV) keratitis (Weiner and Mason, 2019; Clercq, 2007; De Clercq and Li, 2016). Antiviral drugs were then developed to treat various viral infections, including influenza, HSV, hepatitis, human immunodeficiency virus (HIV), and coxsackievirus

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Clean Coal Technologies

Beneficiation, Utilization, Transport Phenomena and Prospective

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Chapter
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Abstract

Water is a vital source for every living organism, and it is very much concerned that it is getting depleted in both surface and groundwater. In the present scenario, the waste from both point and non-point sources increases, thereby increasing pollutants' levels in the water. It is very much needed to this hour that the removal of pollutants with an efficient process could be cost-effective. Many processes have been used to remove

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An Overview of Blockchain Technology in Microgrids

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Abstract—**With the decrement of reserves of fossil energy and the increasing capacity of renewable energy generation, the importance of micro grid based on distributed generations is expanding. Renewable energy sources have emerged as an alternative to meet the growing demand for energy and contribute to sustainable development. The integration of these systems is carried out in a distributed manner through micro grid systems, this provides a set of technical solutions that allows information exchange between the consumers and the distributed generation centers, which implies that they need to be managed optimally and it is highly demanding to secure a reliable balance between energy generation and consumption. To overcome such challenges, peer-to-peer energy trading using block chains on micro grid networks can play a vital role. This paper reviews the concept of existing proposed algorithm that can be useful for energy trading using block chain from both the prosumers and consumers. The outcome of this study proves that if implemented properly this technology would balance the supply and demand locally and also provides the socio-economic benefits to the prosumers and consumers.**

Keywords—Blockchain Technology, Peer to Peer Trading, Proof - Of - Work, Proof –of - stake

I. INTRODUCTION

Renewable energy plays a vital role in meeting energy requirements in both rural and urban areas .The generation of renewable energy and its usage is given a high priority due to its advantages over conventional sources of energy. The necessity to focus on renewable energy based generation is due to the adverse environmental impacts of fossil-based generation. The demand for sustainable energy development is increasing rapidly. Broad usage of renewable energy is important for achieving sustainability in the energy sectors [1].

A micro grid is a combination of distributed energy resources and interconnected loads within clearly defined electrical boundaries that acts as a solitary controllable unit with respect to the grid. A micro grid connects and disconnects from the grid as per the requirement to enable operation in both grid-connected or island mode. With the increasing demand of electricity we cannot rely only on main grid but also need distributed energy sources such as PV solar generation, Wind turbine generation etc. to be connected to the main grid with the help of micro grid to increase the stability as well the reliability of the whole power system. A micro grid can be illustrated as a cluster of loads, decentralized energy resources which are operated in coordination to supply and distribute electricity reliably [2, 3]. In order to facilitate the large number of costumers and prosumers to interact with each other, the decentralized renewable energy system has been placed into the power grid. For autonomous, peer-to-peer exchange, important tasks to be faced are security and control provided in a decentralized manner. Decentralized controlled power exchange system is one of the most challenging issues which balance the energy supply and demand [4]. The energy and information between systems are highly interconnected, and the transparency and security of data must be concerned with the basis of intelligent transactions. Traditional centralized production, distribution, and planning methods may experience significant changes in the era of new energies [5]. The expansion of decentralized renewable energy resources opened the door for a competitive peer to peer energy trading between small scale prosumers and end customers. Consequently, it is expected that peer to peer energy trading will be one of the most important aspect of next generation power systems .Energy trading brings various advantages to utility companies such as increasing the overall efficiency of the grid and reducing operation cost.[6].

There are many methods implemented to have the peer to peer electricity trading which are proposed in this paper. Peer-to-Peer (P2P) energy trading is a new approach of power system operation and control, where people can self generate energy from Renewable Energy Sources (RESs) in offices, factories and on roof tops and share it with each other locally . Blockchain is used as a distributed public ledger technology, which is been widely adopted in the design of new energy trading schemes. However, there are many challenging issues in blockchain-based energy trading, e.g., low efficiency, high transaction cost, and security and privacy issues. To tackle these challenges, many solutions have been proposed [7]. In this paper, the prospects of block chain used in microgrids in the improvement of solar power systems in a decentralized manner are proposed. With implementation of block chain technology for electricity transactions makes the micro grids more flexible by developing mutual trust between the participating agents in terms of electricity delivery and billing.

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Venkata Lakshmi Narayana Komanapalli
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An Efficient Approach for the Detection of Abnormalities in Different Cancerous Images Using TFD Techniques

O. Homa Kesav and G. K. Rajini

Abstract Disease is the conspicuous wellspring of mortality in around the world. The malignant growth which is cancer arises because of unrestrained varieties in a cell. Stringent diagnosis of cancer with explicit procedure is a prerequisite for retaining human lives. The relevant image transforms such as STFT and WT utilize a detection system where the cancerous image features are retained and localize the signal characteristics in different domains. The predetection of malignant growth prompts proper conclusion to either control or fix disease, as at later stages the patient may not react to the treatment. The suspicious tissues are examined and diagnosed with the help of MRI. These filtered pictures can be used to evaluate the destructive cells. The TFD yields appropriate information in the study of non-stationary images. The key objective of TFD representation is to figure out the variations in the frequency substance of images with respect to time. The TFD representation is proposed by STFT and WT to analyze, evaluate and transform the time differing category of images.

Keywords Non-stationary · Time–frequency distribution · STFT · WT

1 Introduction

Malignant growth is depicted by the unusual development of cells in the body. By the aid of blood stream or lymphatic system, it is dispersed to the distinct parts of the body. Cancer is the predominant cause of death worldwide which leads to 8.9 million deaths in 2014 and 9.6 million deaths in 2018 stated by WHO [1]. The typical type of malignant growths causing these deaths is because of breast, thyroid and ovarian diseases.

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BOOK OF ABSTRACTS

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IRON OXIDE-BASED PHOTOCATALYSTS FOR HYDROGEN PRODUCTION AND DYE DEGRADATION UNDER NATURAL SUNLIGHT

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ABSTRACT

Nanomaterials are challenging in simultaneous degradation of pollutants and hydrogen production. This present research work focuses on various visible light active iron oxide nanophotocatalysts for H_2 production and dye degradation. The prepared photocatalysts were characterized for structure (XRD), and morphology (SEM). The efficiency of various iron oxide-based photocatalysts for hydrogen recovery from highly toxic sulphide-containing wastewater is described in this paper. Among the various iron oxide photocatalysts, Yt/Fe_2O_3 shows maximum activity. Effect of operating parameters such as sulphite ion concentration, catalyst dosage, photolytic solution volume, reusability studies were conducted for hydrogen production. The dye degradation studies were conducted for the prepared iron-based catalytic materials using Rhodamine B as the model dye.

Keywords: H_2 production, Yt/Fe_2O_3, Sunlight, dye, Photodegradation.

INTRODUCTION

Industrialization and urbanization pushed us to focus more on research related to environment and energy. Photocatalytic process using direct solar irradiance helps to achieve the generation of renewable energy, H_2 and degradation of pollutants [1]. Research is being done to explore visible light active, stable photocatalyst for maximum hydrogen production and complete mineralization of pollutants. Fe_2O_3 is a promising material for photocatalytic process because of its narrow band gap (2.1 eV), it promises a wide optical absorption in the visible light area. In real-time applications, Fe_2O_3 can increase photocatalytic activity. Incorporation of other metal oxides with Fe_2O_3 is expected to improve the photocatalytic performance several fold. Iron oxide acts as a sinker of photogenerated electrons and hole pairs in it co-catalyst lattice and increases the charge separation and improves the photoactivity [2]. In addition, co-catalyst had maximum active sites than pristine catalyst, thus enhances the hydrogen production as well as degradation [3, 4]. In this study, the iron oxide composites like Al_2O_3/Fe_2O_3, Sm_2O_3/Fe_2O_3 and Y_2O_3/Fe_2O_3 were prepared to recover hydrogen from sulphide wastewater and to destroy the Rhodamine B dye by photocatalysis using natural solar irradiation. Focus was on preparation and characterization of iron oxide based photocatalysts, effect of various factors for achieving maximum hydrogen production and degradation of Rhodamine B dye and its kinetics.

MATERIALS AND METHODS

For synthesis of Pure Iron Oxide, the iron oxide nanoparticles were prepared by combustion process by using natural urea source (Cow urine). For this, 40.4 grams of ferric nitrate ($Fe(NO_3)_3.9H_2O$) was dissolved in 100 mL natural urea solution and stirred for 30 minutes. Then, this homogeneous solution was heated using a hot plate continuously. The urea- iron nitrate solution turns into a transparent viscous gel after an hour of heating which auto ignited to form voluminous foam. Further heating resulted drying of the nanoparticles due to the combustion process.
By following the above combustion process and natural urea fuel, the Iron Oxide: Aluminum Oxide nanoparticles were synthesized. The ferric nitrate and aluminum nitrate ($Al(NO_3)_3.9H_2O$) were taken in equal molar ratio and dissolved separately in 50 mL fuel. After making complete dissolvent, both the solutions are transformed into a single container and mixed thoroughly. Then, the homogeneous solution was heated using a hot plate to precede the combustion process.

For the Iron Oxide: Yttrium Oxide synthesis, equal quantities of ferric nitrate and Yttrium nitrate ($Y(NO_3)_3.6H_2O$) were taken as precursor materials and dissolved separately in 50 ml natural urea. The Iron Oxide: Samarium Oxide synthesis process, the ferric nitrate and Samarium nitrate $Sm(NO_3)_3 \cdot 6H_2O$ were taken in 1:1 ratio as base materials and dissolved in 50 mL natural urea separately.All the processes have yielded very fine particles which were dried and powdered well for further studies and characterization. XRD and SEM analyses were performed.

Photocatalytic solar hydrogen production: Trapezoidal photocatalytic reactor with working volume of 1L was used to recover hydrogen from simulated sulphide wastewater of 0.2M sulphide ion concentration. The reactor is made up of acrylic material. The activities of various iron oxide (Fe_2O_3) photocatalysts were used to check the photocatalytic activity.

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Performance of Static VAR Compensator for Changes in Voltage Due to Sag and Swell

M. S. Priyadarshini and M. Sushama

Abstract The deviations that occur in electrical power supplied by utilities to end users result in voltage decrease termed as sag and increase termed as swell. Due to voltage variations, change is evident for a short duration in voltage, current or frequency. In order to maintain constant voltage to the connected load, compensation devices are used based on flexible AC transmission systems (FACTS) technology. Based on an increase or decrease in voltage, suitable correction action can be taken by power electronic-based devices. The performance of static VAR compensator (SVC), which is a shunt connected FACTS device, is analyzed for voltage sag and swell. The SVC controller scheme, reactive power generated or absorbed, firing pulse generation and modes of SVC operation in MATLAB/Simulink environment are explained.

Keywords Sag · Swell · Thyristor controlled reactor · Thyristor switched capacitor · Static VAR compensator

1 Introduction

Power system is defined as an interconnection between generator and load buses through transmission lines. If any generator is disconnected or taken out for service or maintenance, the lines fed by that generator will be disconnected and must be connected to other generator buses. This results in a change in voltage profile at the buses. Sudden increase in load also affects voltage. To achieve the aim of maintaining constant voltage, proper balance must be maintained between active and reactive power. Electric power supplied by utilities must be free of disturbances and

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A 64-Bit Implementation of Parallel Prefix Adder with Less Hardware Complexity

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***Abstract*— Parallel prefix adders (PPA) are considered effective combinational circuits for performing the binary addition of two multi-bit numbers. These adders are widely used in arithmetic-logic units, which are parts of modern processors, such as microprocessors, digital signal processors, etc. This paper deals with *Kogge-Stone* adder, which is one of the fastest PPA. When performing the schematic implementation, this adder has a large hardware complexity. Therefore, in this work for reducing its hardware complexity the scheme of modified PPA has been developed. The performance parameters considered for the comparative analysis of the presented adders are: the number of logic gates, *Quine*-complexity and maximum delay obtained. Functionality verification and its synthesis are done using Xilinx 13.2.**

Keywords*— *parallel prefix adder (PPA); Kogge-Stone adder; modified parallel prefix adder; the number of logic gates; Quine-complexity; maximum delay; prefix tree; schematic nodes

I. Introduction

The hardware implementation of binary addition is a fundamental architectural component in many processors, such as microprocessors, digital signal processors, mobile devices and other hardware applications [**Error! Reference source not found.**]. In these systems when building arithmetic logic unit (ALU), adders play an important role for performing the basic arithmetic operations, such as addition, subtraction, multiplication, division, etc. [**Error! Reference source not found.**]. Therefore, the hardware implementation of an effective adder is necessary to increase the performance of ALU and, consequently, the processor itself as a whole. Currently, a parallel prefix adder (PPA) is considered effective adder for performing the addition of two multi-bit numbers. Circuit complexity and the speed of PPA are important parameters at the stage of efficient hardware implementation and, therefore, in recent years various types of PPA with different characteristics of the parameters have been developed while performing the binary addition. However, for estimation of hardware costs this adder has a great number of logic gates and *Quine*-complexity used in the schematic implementation. Therefore, in the present work for reducing its hardware complexity a modified parallel prefix adder is developed. Then, the comparison of the two presented adders is made by the following parameters: the number of logic gates, *Quine*-complexity, as well as the delay obtained by simulation in *Quartus II* CAD environment based on FPGA Altera *EP2C15AF484C6*. A perspective architecture is proposed for schematic implementation of various PPA. And derivation of the formulas is also described for computing the hardware characteristics which are dependent on the bit width of input operands of the presented adders.

II. Architecture Of The Parallel Prefix Adder

Parallel prefix adder (PPA) is a multi-bit carry-propagate adder which is used for parallel addition of two multi-bit numbers. PPA extend the generated and propagated logic of the carry look-ahead adder to perform addition even faster [4]. As the basic schematic structure of the various PPA, perspective architecture is analyzed, it consists of three stages (Figure 1) [5]: pre-processing stage, prefix computation stage and final processing stage. Let consider each stage in more detail.

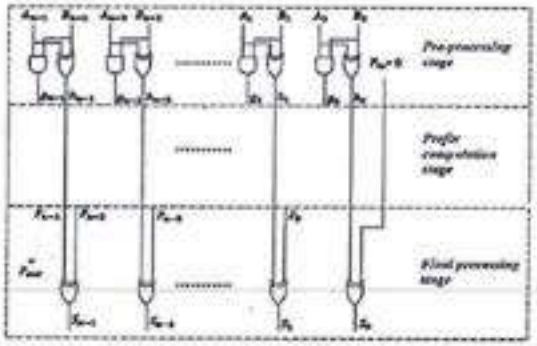

Fig. 1. Architecture of the parallel prefix adder

In this paper *Kogge-Stone* adder [3] is investigated, which is one of the known effective fastest PPA. *Kogge-Stone* is widely and efficiently used. Such an adder has minimum delay

At the pre-processing stage, carry-generate g_i and carry-propagate h_i signals are computed for each pair of input

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RESEARCH ARTICLE OPEN ACCESS

Self-Cleaning Surface-Coat of Micro Titanium Dioxide on Hardened Cement Mortar Surfaces Irradiated With Sunlight

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Abstract:

One of the common problem happening is the deterioration of building facades due to increase in urban environmental pollution. Self cleaning cementitious materials have come under spotlight as a intelligent building materials and green materials for sustainable environment. Titanium dioxide is a promising photo catalytic material in degradation of many organic pollutants. This paper illustrates the self cleaning performance of titanium dioxide (size range 130 nm) as a coating applied on hardened cement mortar surfaces. The prepared samples i,e micro TiO_2 coated discs are completely immersed in earlier prepared Rhoda mine B solution(3 mg/l) having a wave length peak at 554.8 nm and exposed to sunlight. In the present study Rhoda mine B dye used as a decolourised indicator under sunlight. The research work done by applying different dosages of TiO_2 on hardened surfaces showed good photocatalytic efficiency as well as its potential application in prevention of building facades due to urban environmental pollution.

Keywords: Micro TiO_2, photo catalysis, Rhoda mine B, Sunlight, Environmental application

1. Introduction

The potential of TiO_2 as a catalyst was discovered by Fujishima and Honda in 1972. TiO_2 is a semiconductor, which has three crystal arrangements anatase, rutile, and brookite, of the three research has shown that titanium dioxide in the anatase exhibits the highest photo activity as a environmental depollutant [1].TiO_2 as a photocatalyst seems to be very promising material due to its several advantages like Strong oxidising power, Anti-bacterial properties, Self-cleansing & De-polluting capabilities, non -toxic, chemical stability, high refractive index [2].When the TiO_2 cement surfaces either hydrophilic or hydrophobic are exposed to the irradiation, the catalyst gets photo excited and then the photocatalytic process begins [3]. TiO_2 is recently found to be an excellent photocatalyst to be used in pavement engineering for reducing vehicle emission pollutants [4]. Pollutants from vehicle exhaust adsorb to the pavement. The TiO_2 coating on the pavement surface activates with the ultraviolet sunlight to break down the pollutants.

Ming Zhi Guo et al.[5] demonstrated an effective way to incorporate nano TiO_2 in photo catalytic cementitious materials by using three TiO_2 sprayed methods .spray A method in which surface layers were sprayed with TiO_2 solution 30 times after mechanical compacting. Spray AB method in

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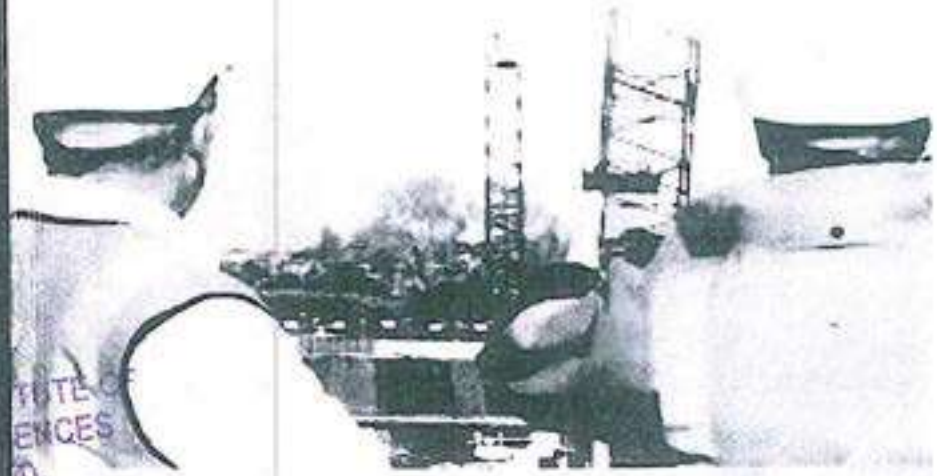

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14 TRANSISTOR FULL ADDER CIRCUIT USING 4 TRANSISTOR XOR GATE AND TRANSMISSION GATE

S.NARENDRA[1], A.MAHESWARA REDDY[2], S.SALEEM [3], K.M.HANEEF [4]

Abstract:

A rapid growth is been observed in the area of Integrated Circuits (IC) technology. All the ICs are to be designed in an optimized way so that they meet all the requirements of being faster, occupying less area and reduced power consumption. One of the circuits which occupy most of ICs is ALU which is a combination of arithmetic and logic units. Of the arithmetic units two are most important which are the adders and multipliers. This paper describes an efficient method to design full adders which is the basic unit of adders in ALUs.

Key words: **ALU, Logic gates, Pass Transistor Logic, Transmission gate.**

I. INTRODUCTION

Now days all the systems are built on an upcoming technology called System on Chip (SoC) in which all the components and peripherals have been built on a single chip which increases the complexity of the system. VLSI plays an important role in the development of such ideas.

Initially the electronics started their evolution with the invention of vacuum tubes. But with the help of Vacuum tubes only the movement of electrons was studied. After vacuum tubes transistors and diodes were introduced. But for larger circuits it was difficult to fabricate them in a board as they occupied larger space and consumed more power. Also it was difficult for the designers to identify the wiring and routing faults which occurred in such circuits. This led to the invention of Integrated Circuits by Jack and Kilby in which more number of transistors were integrated on a single chip. Initially 3 to 30 transistors were fabricated in a single chip which is known as Small Scale Integration (SSI). Then about 30 to 300 transistors were developed in a single chip which is known as Medium Scale Integration. All the above events happened in 1940S.

Colloquially Moore's law stated that the number of transistors on a single chip doubles each and every eighteen months. Further developments were LSI (300 to 3000 transistors in a single chip), VLSI (3000 to 30000 transistors in a single chip) and now it the upcoming technology is the ULSI with the fabrication of millions of transistors in a single chip. Also Moore's law found a drawback that in even less than eighteen months the number of transistors in a single chip got doubled.

Also circuits were introduced to do the arithmetic and logic operations. Initially logic operations such as AND, OR, NOT, NAND, NOR, EX-OR were done by LSI ICs. And circuits for doing arithmetic operations such as addition subtraction and multiplication were developed which made the field of signal processing and communication field involving arithmetic operations to glow more.

Half adder was designed to add two one bit numbers and when carry arose, that lead to the development of full adders which added three one bit numbers and produced. Full adder acts as the basic block of all adders which are used to perform multi bit additions.

RESEARCH ARTICLE OPEN ACCESS

DESIGN AND ANALYSIS OF CONFIGURABLE MULTIPLIERS USING DUAL QUALITY 4:2 COMPRESSORS

M. Sree vidya[1], P.Anjaneya[2], O. Homa kesav[3] ,G.K.Rajini[4]

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Abstract:

Multiplier plays a vital role in many applications such as digital image processing, digital signal processing etc...so it is important to design the multiplier with low power consumption and reduced delay. In order to reduce this factor we design the multiplier using four 4:2 compressor and these compressors has a dual quality property and this property is used to switch between the exact and approximate modes. When it operates at approximate mode it reduces the power consumption and area at the cost of low accuracy. During approximate and exact mode each of these compressors has different power consumption and delays but only at approximate mode these compressors has its own level of accuracy. Hence these compressors are used in the design of parallel multiplier .These parallel multipliers provides configurable multiplication whose accuracy may change dynamically during the run time. We implement these compressors in a 32 bit dada multiplier which is evaluated in a 45 nm standard CMOS technology.

Index Terms: Power, 4:2 compressors, Accuracy, Approximate computing, Configurable, Delay

1. INTRODUCTION

The most commonly used techniques for the generation of approximate arithmetic circuits are truncation, voltage over scaling (VOS) and simplification of logic .Extensive research has been conducted on approximate address providing significant gains in terms of area and power while exposing small error. Approximate hardware circuits, contrary to software approximations, offer transistors reduction, lower dynamic and leakage power, lower circuit delay, and opportunity for downsizing.

Motivated by the limited research on approximate multipliers, compared with the extensive research on approximate adders, and explicitly the lack of approximate techniques targeting the partial product generation, we introduce the partial product perforation method for creating approximate multipliers. We omit the generation of some partial products, thus reducing the number of partial products that have to be accumulated; we decrease

RESEARCH ARTICLE OPEN ACCESS

A Reconfigurable FIR Filter Architecture to Trade off Filter Performance for Dynamic Power Consumption

V.Ruth Havila[1], O.Homa Kesav [2], P.Anjaneya[3] , G.K.Rajini[4]

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Abstract:

An architectural approach to design low power reconfigurable finite impulse response (LPRFIR) filter. The LPRFIR is well suited when the filter order is fixed and not changed for particular applications and efficient trade-off between power savings and filter performance can be implemented using the proposed architecture. Generally, FIR filter has large amplitude variations in input data and coefficients. Considering the amplitude of both the filter coefficients and inputs, proposed FIR filter dynamically changes the filter order. Mathematical analysis on power savings and filter performance degradation and its experimental results shows that the proposed approach achieves significant power savings without seriously compromising the filter performance. The power savings is up to 20.5% with minor performance degradation and the area overhead of the proposed scheme is less than 5.3% compared to the conventional approach.

Keywords: Approximate filtering, low power filter, reconfigurable design, high speed filter

1. INTRODUCTION

THE demand for low power digital signal processing (DSP) systems has increased due to explosive growth in mobile computing and portable multimedia applications. One of the most widely used operations performed in DSP is finite impulse response (FIR) filtering. The input-output relationship of the linear time invariant (LTI) FIR filter can be expressed as the following equation:

$$Y(n)=\sum_{k=0}^{N-1} c_k x(n-k) \quad (1)$$

Where N represents the length of FIR filter, c kthekth coefficient, and x(n – k) the input data at time instant(n-k) . In many applications, in order to achieve high spectral containment and/or noise attenuation, FIR filters with fairly large number of taps are necessary. Many

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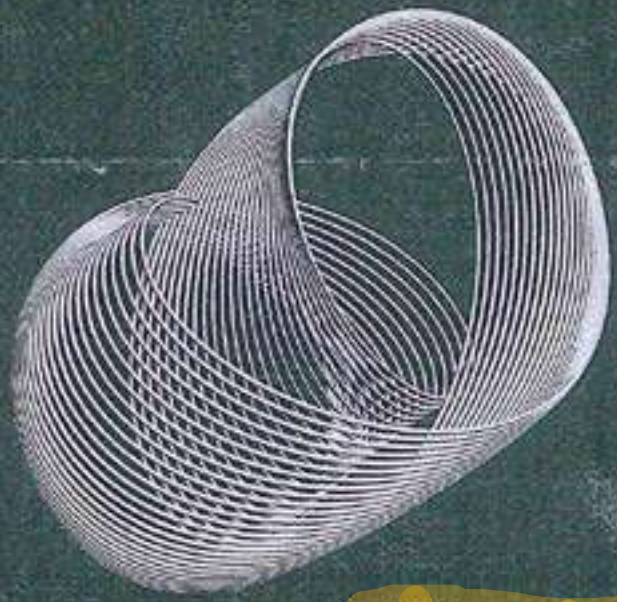

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Dr. T. Ravindra Reddy

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For Undergraduate Courses of All Universities

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A Survey on Wind Energy, Load and Price forecasting

(Forecasting Methods)

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***Abstract*— The wind energy has an upward trend to continue over several decades, with the improvement of its turbine technology and reduction of energy production costs. Due to its unpredictable wind behavior and weather patterns, it may pose many problems including grid voltage balancing, synchronization, capital cost expenditure etc. So, there would be a definite need forecast the wind energy, its load and price. The use of these forecasting techniques may cause reduce the capital cost, installation and maintenance etc., Hence, in this article an attempt has been made to review the forecasting techniques for wind energy, load and price also it tried to explores the best possible methods for forecast the behavior/pattern.**

Keywords*— *wind power; load forecasting; price forecasting; wind energy forecasting

I. INTRODUCTION (*HEADING 1*)

Load forecasting is defined as an estimation, or a prediction of electrical energy will be needed by the energy consumers and other utility systems in nearby future. In any electrical power system load forecasting is a control and integral process in the planning and operation of electric utilities [6]. It plays a key role in reduction of generating cost in generating stations. For knowing the future load demand, one should follow the prediction/forecasting techniques. It is preplanned process about sharing of loads for the coming years. It is helpful in avoiding the shortages/outages in the utility systems and saves price for generating companies as well as utility systems.

Electricity price forecasting (EPF) is defined as the process of using mathematical models to determine what electricity prices will be in future years based on the consumption of electricity [3]. After load forecasting, price could be decided by performing the price forecasting. Based on the time horizons both load and price forecasting are classified into 3 types they are short term (one hour to one week), medium term (one month to a year) and long term (over one year).

The time factors, weather data and consumer classes would be considered for short term forecasting. Time factors includes the time of year, the day of the week and an hour of the day. There are important differences in load consumption between weekdays and weekends. In weekdays, the consumption of load would be high and where as in weekends the load consumption would be less comparatively. Holidays are more difficult to forecast than the non-holidays because of their relative infrequent occurrence. Also, weather conditions plays a vital role in load forecasting. Temperature and humidity are most commonly used load effectors [7]. For this factor some organizations found, THI (Temperature-Humidity Index) and WCI (Wind Chill Index) are broadly used. THI is used for the measurement of summer heat and WCI is used for the measurement of cold stress in winter.

II. LOAD FORECATING METHODS

A. Short Term Forecasting Method

Short term forecasting techniques ranging from very simple extrapolation to high complex time series techniques has been developed in [10], by employing the combination of techniques that gives aggregate annual forecast.

(i). Similar Day Approach

This method is based on searching historical data for days within one, two or three years with some characteristics to the forecast day [10-11]. In that, it includes the weather details, day of the week and then the load of the similar day is considered. With this approach, the forecast could be easy for in any practical power systems and final forecasting error is comparatively low. The main disadvantage of this method is, if any weather conditions are affected in the previous similar day then it miss matches the present day weather conditions. The flow chart of this approach is shown in fig.1(a).

(ii). Time Series Method

Time series method uses qualitative forecasting techniques, which are based on analysis of historical data, and can be used to forecast future data points. Time series methods make forecasts based on historical patterns. It uses time as independent variable to produce demand and measurements are taken at successive periods. These measurements may be taken

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Systematic Design of High-Speed and Low-Power Domino Logic

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Abstract: *Dynamic Domino logic circuits are widely used in modern digital VLSI circuits. Because it is simple to implement, low cost designs in CMOS Domino logic are presented. Compared to static CMOS logic, dynamic logic offers good performance. Wide fan-in logic such as domino circuits is used in high-performance applications. Domino gates typically consume higher dynamic switching and leakage power and display weaker noise immunity as compared to static CMOS gates. This paper compares static CMOS, domino logic design implementations. For the comparison of static CMOS and DOMINO logic we will see various design of Domino logic gates and as well as design of logic circuits using Domino logic gates.*

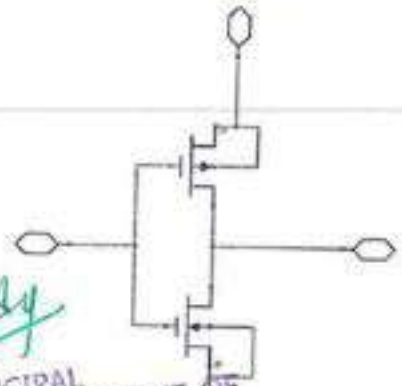
Keywords *– Dynamic; Domino; CMOS; Very Deep submicron technology; High speed; Low Power.*

I. INTRODUCTION

Dynamic circuits are widely used in custom circuit design to achieve higher speed, smaller area and potentially lower power consumption due to glitch -free operation. There are also difficulties in designing and verifying this class of circuits However, Domino logic circuits can implement only non-inverting logic; the synthesis of a Domino logic circuit typically involves the conversion to a unate representation from the original binate logic network. Synthesis of domino circuits is more complicated than that of static circuits. The added complexity is due to domino log ic's monotonic nature which forces it to implement only non-inverting functions. Therefore, domino logic can only be mapped to a network of non-inverting functions, where needed logic inversions must be performed at either primary inputs and/or primary outputs. Dynamic logic is over twice as fast as normal logic; it uses only fast N transistors. Static logic is slower because it uses slow P transistors to compute logic. Dynamic logic is harder to work, but if we need the speed there is no other choice. There are also difficulties in designing and verifying this class of circuits. Dynamic circuitry can become highly sensitive to clock skew, charge sharing etc. Do mino logic has created a substantial interest due to its performance and CMOS power consumption. It runs 1.5 - 2 times faster than static CMOS logic because dynamic

II. RELATED WORK

Dynamic logic (or sometimes clocked logic) is a design methodology in combinational logic circuits, particularly those implemented in standard CMOS logic .Standard CMOS logic has the disadvantages of increased area, complexi-ty and delay. Standard CMOS logic is built on transistors. The input is same to both the PMOS and NMOS transistors.



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Carry Select Adder Using Common Boolean Logic

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***Abstract:** In electronics, adder is a digital circuit that performs addition of numbers. To perform fast arithmetic operations, carry select adder (CSLA) is one of the fastest adders used in many data- processing processors. The structure of CSLA is such that there is further scope of reducing the area, delay and power consumption. Simple and efficient gate – level modification is used in order to reduce the area, delay and power of CSLA. Based on the modifications, 8-bit, 16-bit, 32-bit and 64-bit architectures of CSLA are designed and compared. In this paper, conventional CSLA is compared with Modified Carry select adder (MCSLA), Regular Square Root CSLA (SQRT CSLA), Modified SQRT CSLA and Proposed SQRT CSLA in terms of area, delay and power consumption. The result analysis shows that the proposed structure is better than the conventional CSLA.*

***Keywords:** Adder, Carry select Adder (CSLA), Modified CSLA (MCSLA), Square Root CSLA (SQRT CSLA), Data rocessing processors.*

I.INTRODUCTION

In many computers and other kind of processors, adders are not only used in the arithmetic logic unit, but also in other parts of the processor, where they are used to calculate addresses, table indices and similar applications. Some other applications of adders are in Multiply – Accumulate (MAC) structures. Adders are also used in multipliers, in high speed integrated circuits and in digital signal processing to execute various algorithms like FFT, IIR and FIR. Now a days, design of low power, area efficient high speed data path logic systems are the most substantial areas in the research of VLSI design.

On the basis of requirements such as area, delay and power consumption some of the complex adders are Ripple Carry Adder, Carry look-Ahead Adder and Carry Select Adder. Ripple Carry Adder (RCA) shows the compact design but their computation time is longer. Time critical applications make use of Carry Look-Ahead Adder (CLA) to derive fast results but it leads to increase in area. But the carry select adder provides a compromise between the small areas but longer delay of RCA and large area with small delay of Carry Look Ahead adder.[1]

This paper presents a comparative analysis of various adders and proposed design of SQRT CSLA by sharing Common Boolean Logic and modified CSLA using Binary to Excess-1 Converter (BEC). Both these adders show less area, delay and power than other adders.

This paper is organized as follows: In section II literature survey is shown, section III deals with modified CSLA, section IV explains Regular SQRT CSLA and Modified SQRT CSLA and section V explains about Proposed SQRT CSLA using common Boolean logic. Results are analysed in section VI and section VII concludes. Section VIII tells about future scope.

II. LITERATURE SURVEY

Ripple Carry Adder consists of cascaded "N" single bit full adders. Output carry of previous adder becomes the input carry of next full adder. Therefore, the carry of this adder traverses longest path called worst case delay path through N stages. Fig. 1 shows the block diagram of ripple carry adder. Now as the value of N increases, delay of adder will also increase in a linear way. Therefore, RCA has the lowest speed amongst all the adders because of large propagation delay but it occupies the least area. Now CSLA provides a way to get around this linear dependency is to anticipate all possible values of input carry i.e. 0 and 1 and evaluate the result in advance. Once the original value of carry is known, result can be selected using the multiplexer stage. Therefore the conventional CSLA makes use of Dual RCA's to generate the partial sum and carry by considering input carry C_{in}=0 and C_{in}=1, then the final sum and carry are selected by multiplexers. Fig. 2 shows the 16-bit Conventional CSLA.

The conventional CSLA is area consuming due to the use of dual RCA's.

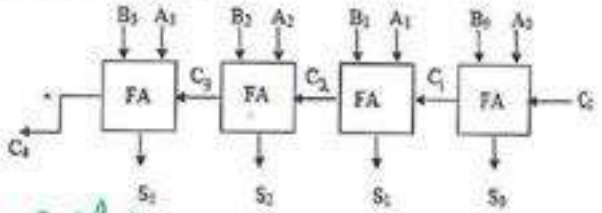

Fig. 1 4-bit Ripple Carry Adder

The basic idea of this work is to use Binary to Excess-1 converter (BEC) instead of RCA with C_{in}=1 in conventional CSLA in order to reduce the area and power. [2] [3] BEC uses less number of logic gates than

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Adder Enhancement Techniques

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Abstract: *Adders are one of the most widely digital components in the digital integrated circuit design and are the necessary part of digital signal processing (DSP) applications. With the advances in technology, researchers have tried and are trying to design adders which offer either high speed, low power consumption, less area or the combination of them. The addition of the two bits is very based on the various speed-up schemes for binary addition, a comprehensive overview and qualitative evaluation of the different existing basic adder architectures are given in this paper. In addition , their comparison is performed in thesis for the performance analysis. We will synthesize the adders –Ripple Carry adder, Carry skip adder, Carry select adder and Carry look –ahead Adder, in ISE XILINX 13.2 by using HDL - Verilog and will simulate them in same tool. We will compare above mentioned adders in terms of delay, Slices Used and Look up tables used by the adders architecture.*

Key words :*Ripple Carry Adder, Carry Look Ahead adder, Carry Save adder*

INTRODUCTION

In many computers and other kind of processors, adders are not only used in the arithmetic logic unit, but also in other parts of the processor, where they are used to calculate addresses, table indices and similar applications. Some other applications of adders are in Multiply – Accumulate (MAC) structures. Adders are also used in multipliers, in high speed integrated circuits and in digital signal processing to execute various algorithms like FFT, IIR and FIR. Now a days, design of low power, area efficient high speed data path logic systems are the most substantial areas in the research of VLSI design.

On the basis of requirements such as area, delay and power consumption some of the complex adders are Ripple Carry Adder, Carry look-Ahead Adder and Carry Select Adder. Ripple Carry Adder (RCA) shows the compact design but their computation time is longer. Time critical applications make use of Carry Look-Ahead Adder (CLA) to derive fast results but it leads to increase in area. But the carry select adder provides a compromise between the small areas but longer delay of RCA and large area with small delay of Carry Look Ahead adder.[1]

This paper presents a comparative analysis of various adders and comparison in terms of area and delay

RIPPLE CARRY ADDER

A ripple adder that adds two N-bit operands requires N full adders. The speed varies linearly with the word length. The RCA implements the conventional way of adding two numbers. In this architecture the operands are added bitwise from the least significant bits (LSBs) to the most significant (MSBs), adding at each stage the carry from the previous stage.

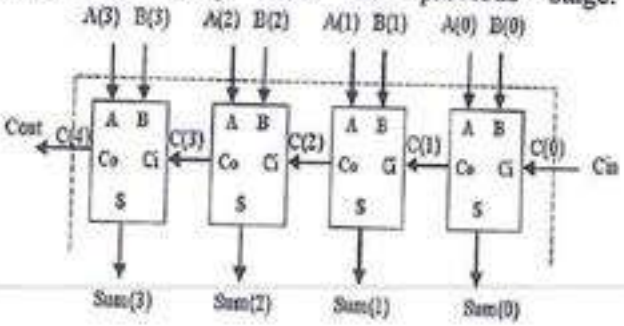

Fig : 4-bit Ripple Carry Adder

Thus the carry out from the FA at stage i goes into the FA at stage (i +1), and in this manner carry ripples from LSB to MSB (hence the name of ripple carry adder). The layout of a RCA is simple, which allows fast design time. However, RCA is relatively slow, since each full adder must wait for the carry bit which is coming from the